Product Application Specification For 1.0mm Pitch Cool Edge Series Connector (Compatible with PCIe)

REVISION RECORD

REV	PAGE	DESCRIPTION	ECN#	DATE	Prepare By
A	8	First Release	CD----	2021-01-08	JERRY
B	12	Update File Title	CD2369	2021-01-25	Jun.Fan
C	12	Update Add-in Card Layout for Gen5	CD2675	2021-06-04	Jun.Fan
D	12	Update PN	ELX-CD-F2998-1	2022-04-14	Mark.qiu
E	12	Change the PN Description	ELX-CD-F2998-1	2022-04-15	Mark.qiu

Prepared by :	Date:	Approved by :	Date:
(Product Engineer)		(Engineering Manager)	

TABLE OF CONTENT:

1. OBJECTIVE

This specification provides information and requirements for customer application of the 1.0mmPitch Cool Edge Connector. It is intended to provide general guidance for process development. It should be recognized that no single process will work under all customer applications and the customers should develop processes to meet individual needs. However, if the processes vary from the recommended one, Amphenol cannot guarantee acceptable results.

2. SCOPE

This specification provides information and requirements regarding application of 1.0mm Pitch Cool Edge Connector to printed circuit boards (PCB). The connectors are designed for mother/daughter board applications and compatible with standard PCIe interface.

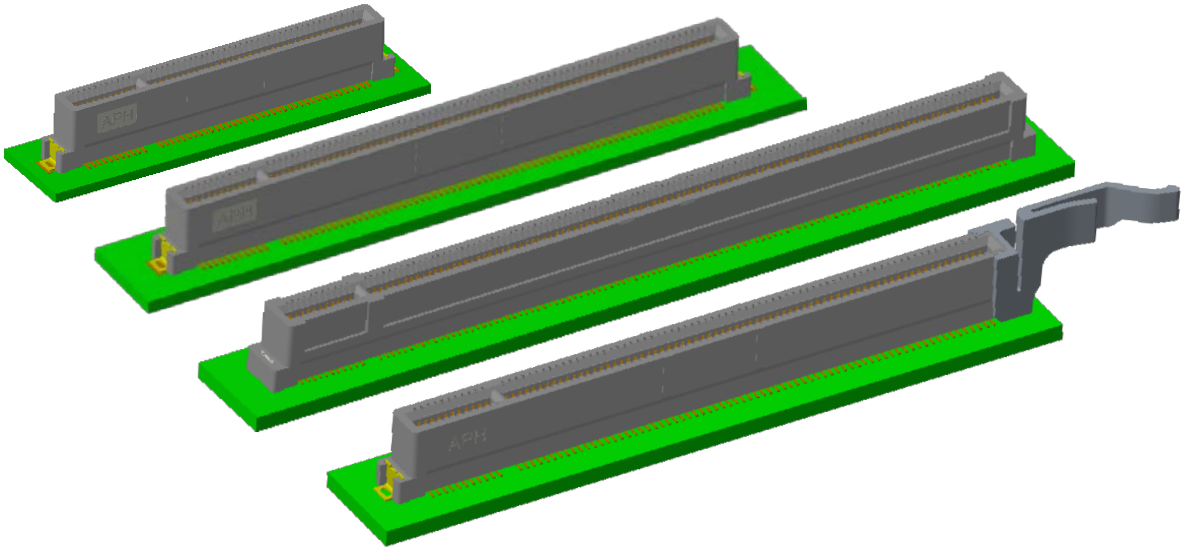


Figure 1: 1.0mm Pitch Cool edge connector

3. DRAWING AND APPLICABLE DOCUMENTS

- Amphenol Product Specification SCE009
- Application Amphenol Customer Drawings

Amphenol product drawings and specifications are available by accessing the Amphenol website or contacting the Amphenol Technical Service. In the event of a conflict between this specification and the product drawing, the drawing takes precedence. Customers should refer to the latest revision level of Amphenol product drawings for appropriate product details.

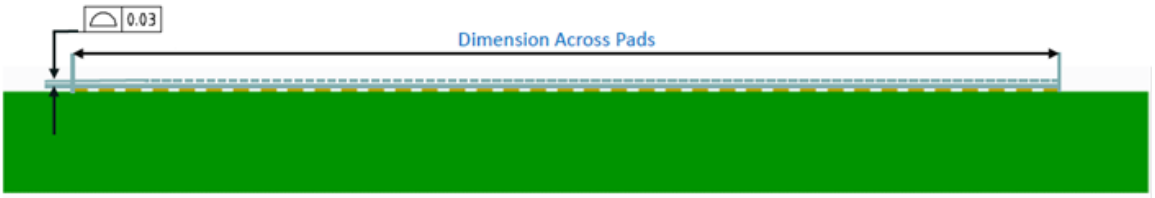
4. PC BOARD REQUIREMENTS

4.1 MATERIAL AND THICKNESS

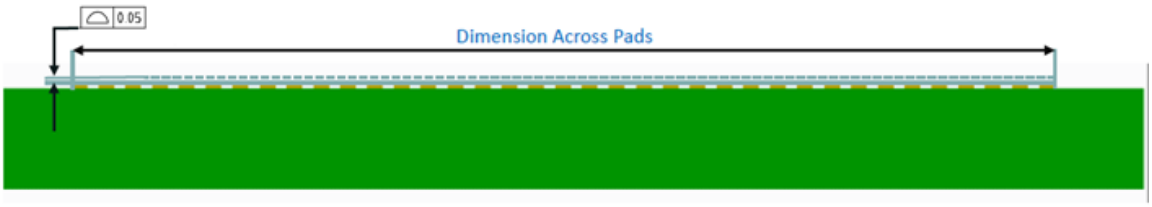
The pc board material shall be glass epoxy (FR4 or G-10) or more advanced material.
The recommended minimum pc board (mother board) thickness shall be 1.57mm.

4.2 PC BOARD HIGH TEMPERATURE PAD CO-PLANARITY

Maximum allowable bow (co-planarity) shall be 0.03mm across the length of the pad area In the case of 0.13mm thick solder paste.



Maximum allowable bow (co-planarity) shall be 0.05mm across the length of the pad area In the case of 0.15mm thick solder paste



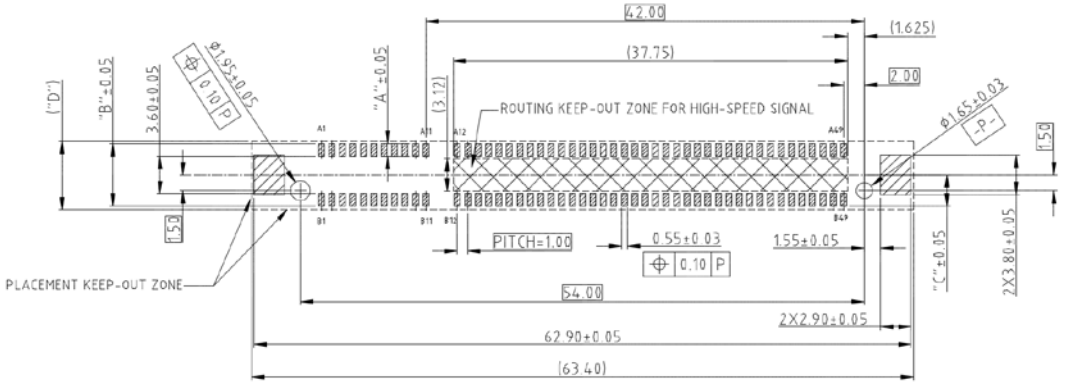
4.3 SURFACE TREATMENT

The recommended surface treatment for soldering pads is immersion plating Tin, as the solder tails always are Tin plated.
The recommended surface treatment for add-in card is gold plating, as the connector contact area always is gold plated.

4.4 LAYOUT

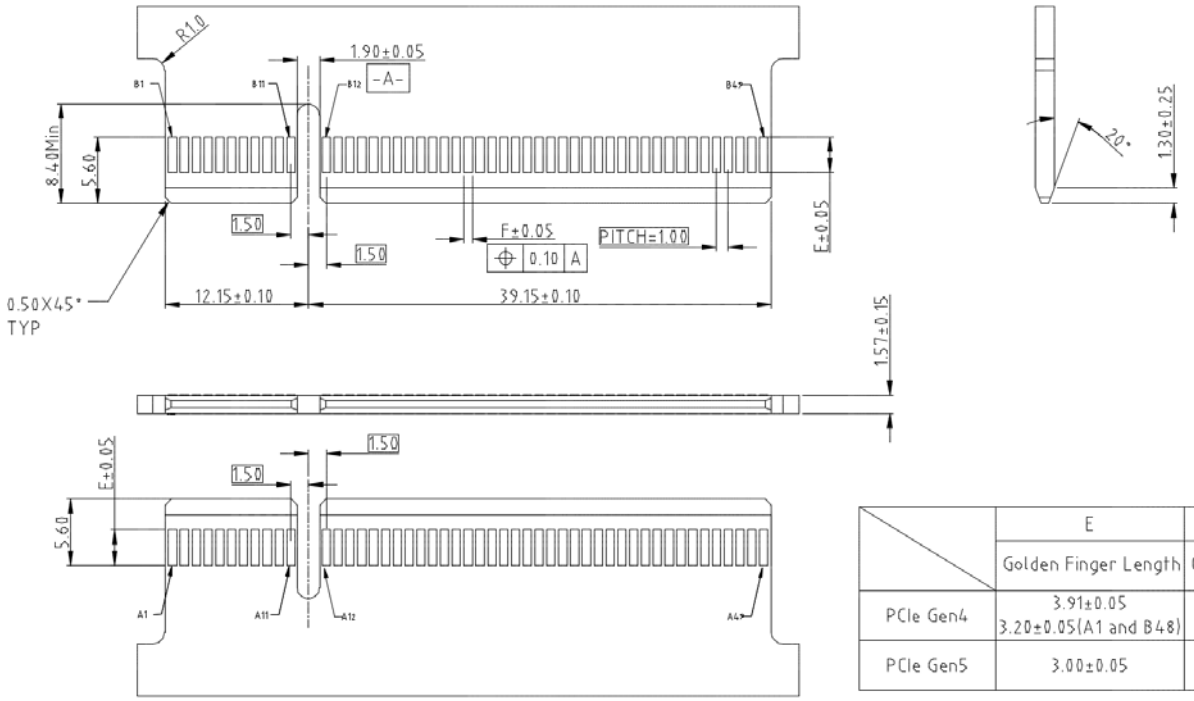
The holes for the connector assembly must be precisely located to ensure proper placement and optimum performance of the connector assembly. Recommended general holes, pads, dimensions, and tolerances are provided in Figure 2 to 9. It's a general layout; please refer to appropriate sales drawing for recommended PCB layout for each part.

4.4 .1 CEE0098X014XXXX



	A	B	C	D
SHORTER TAIL	1.20	6.00	3.00	6.55
STD TAIL	1.90	7.40	3.70	7.95

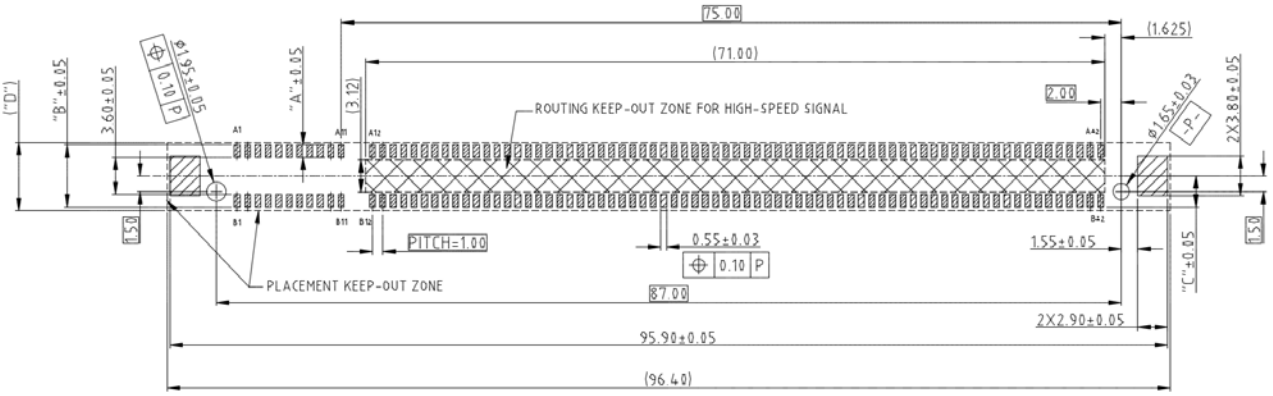
GENERAL PCB LAYOUT FOR MOTHER BOARD
(Your configuration may vary)
FIGURE 2



	E	F
	Golden Finger Length	Golden Finger Width
PCIe Gen4	3.91±0.05 3.20±0.05(A1 and B48)	0.70±0.05
PCIe Gen5	3.00±0.05	0.60±0.05

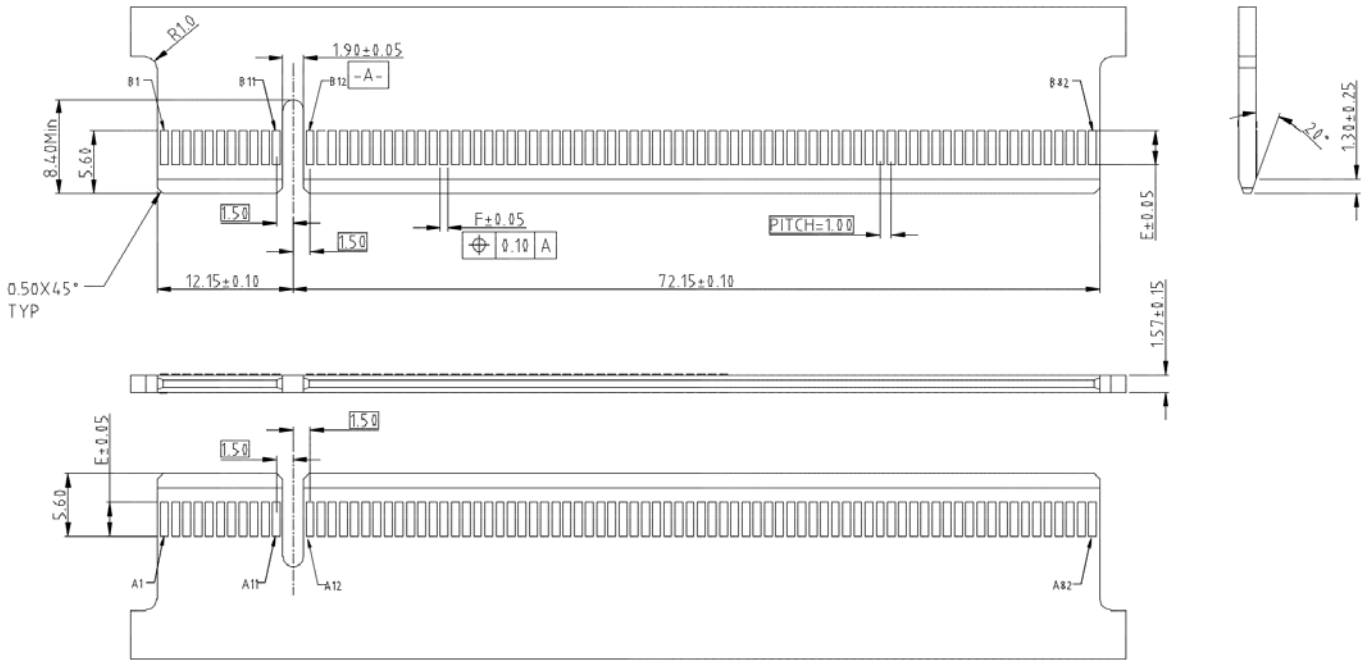
GENERAL LAYOUT FOR ADD-IN CARD
(Compatible with PCIe CEM industrial standard)
FIGURE 3

4.4 .2 CEE0164X014XXXX



	A	B	C	D
SHORTER TAIL	1.20	6.00	3.00	6.55
STD TAIL	1.90	7.40	3.70	7.95

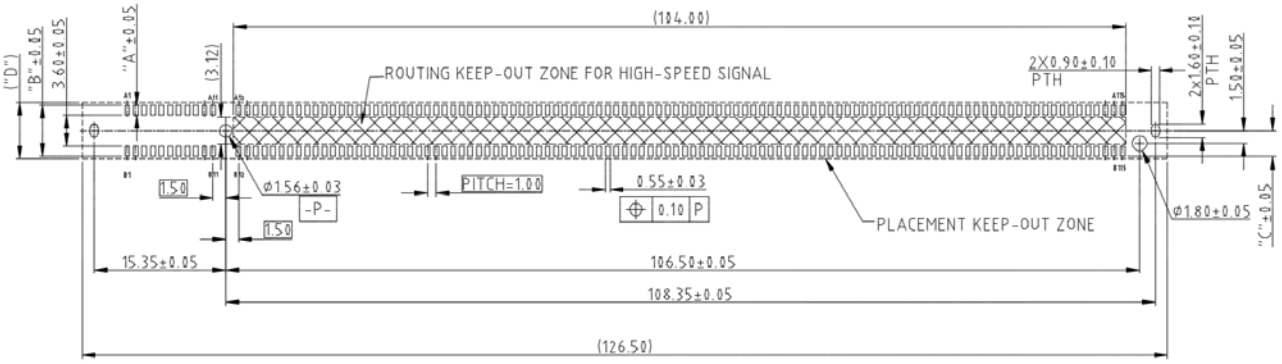
GENERAL PCB LAYOUT FOR MOTHER BOARD
(Your configuration may vary)
FIGURE 4



	E	F
	Golden Finger Length	Golden Finger Width
PCIe Gen4	3.91±0.05 3.20±0.05(A1 and B48)	0.70±0.05
PCIe Gen5	3.00±0.05	0.60±0.05

GENERAL LAYOUT FOR ADD-IN CARD
(Compatible with PCIe CEM industrial standard)
FIGURE 5

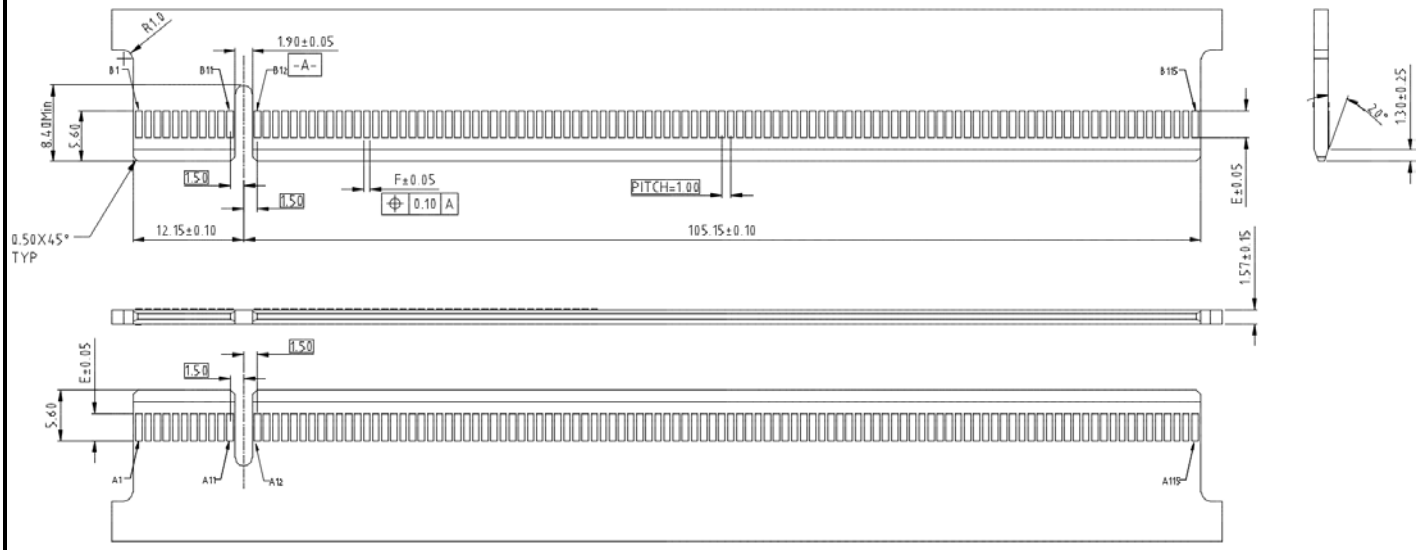
4.4 .3 CEE0230X014XXXX



	A	B	C	D
SHORTER TAIL	1.20	6.00	3.00	6.55
STD TAIL	1.90	7.40	3.70	7.95

GENERAL PCB LAYOUT FOR MOTHER BOARD
(Your configuration may vary)

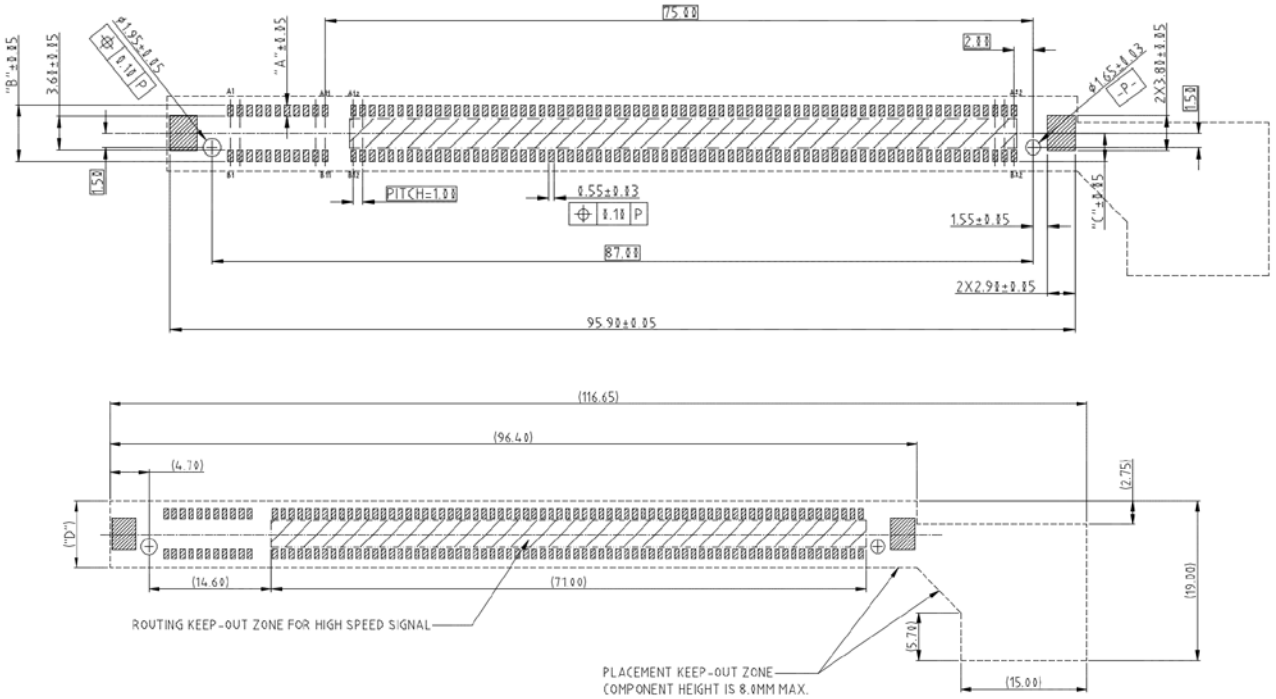
FIGURE 6



	E	F
	Golden Finger Length	Golden Finger Width
PCIe Gen4	3.91±0.05 3.20±0.05(A1 and B48)	0.70±0.05
PCIe Gen5	3.00±0.05	0.60±0.05

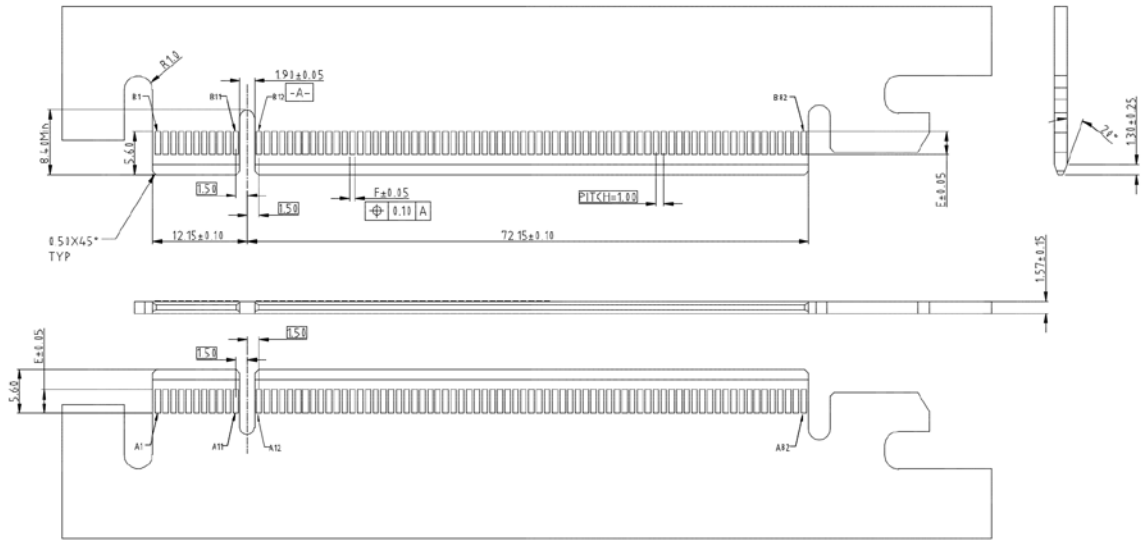
GENERAL LAYOUT FOR ADD-IN CARD
FIGURE 7

4.4 .4 CEE0164X114XXXX



	A	B	C	D
SHORTER TAIL	1.20	6.00	3.00	6.55
STD TAIL	1.90	7.40	3.70	7.95

GENERAL PCB LAYOUT FOR MOTHER BOARD
(Your configuration may vary)
FIGURE 8



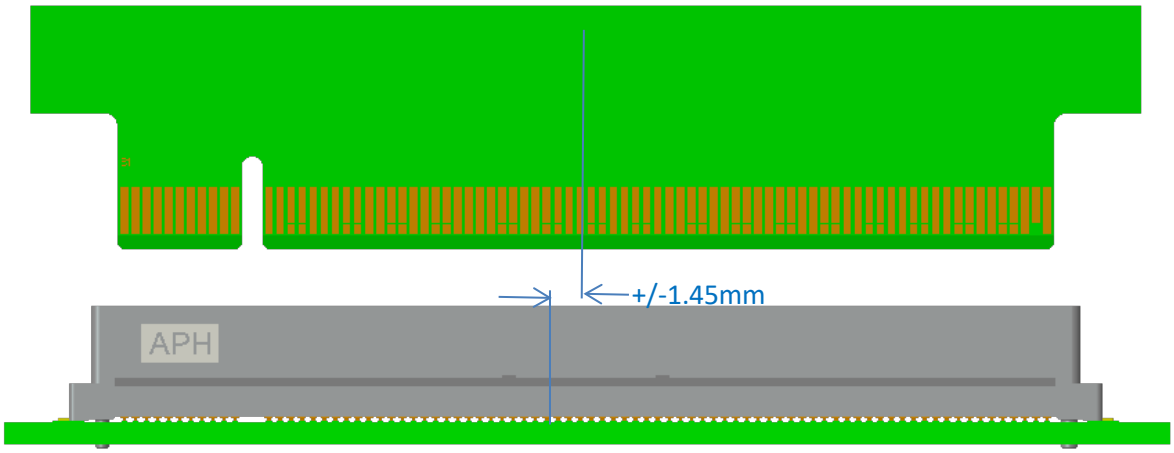
	E	F
	Golden Finger Length	Golden Finger Width
PCIe Gen4	3.91±0.05 3.20±0.05(A1 and B48)	0.70±0.05
PCIe Gen5	3.00±0.05	0.60±0.05

GENERAL LAYOUT FOR ADD-IN CARD
(Compatible with PCIe CEM industrial standard)
FIGURE 9

5. MATING AND ALIGNMENT

5.1 GUIDING FEATURES IN “X” DIRECTION

Nominal misalignment correction in “X” direction:+/-1.45mm

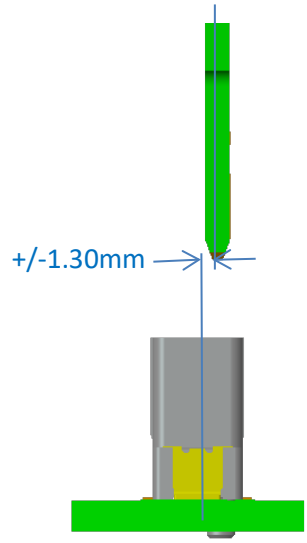


Notes:

This is a generic calculation based on Amphenol Connector dimension and may be impacted by the PCB manufactures capabilities.

5.2 GUIDING FEATURES IN “Y” DIRECTION

Nominal misalignment correction in “Y” direction:+/-1.30mm



Notes:

This is a generic calculation based on Amphenol Connector dimension and may be impacted by the PCB manufactures capabilities.

5.3 WIPE LENGTH

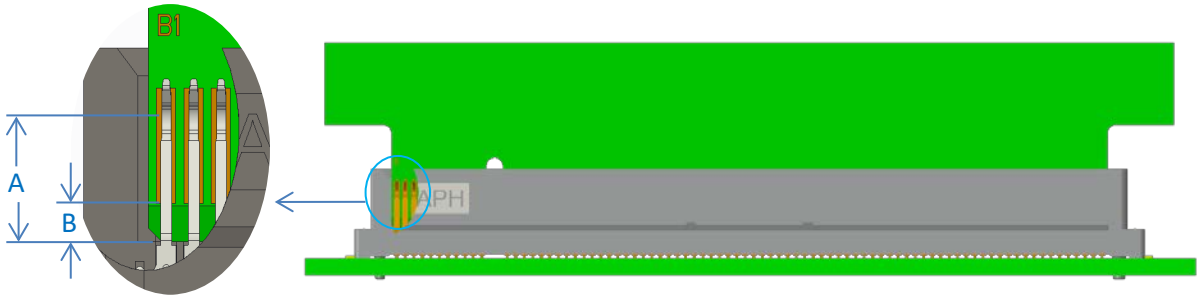
A=contact area to housing slot bottom

B=Gold finger lower edge to PCB edge

General signal pins(Gen 4): A=4.40mm ;B=1.69mm; Wipe length=A-B=2.71mm

Detection pins(Gen 4): A=4.40mm ;B=2.40mm; Wipe length=A-B=2.00mm

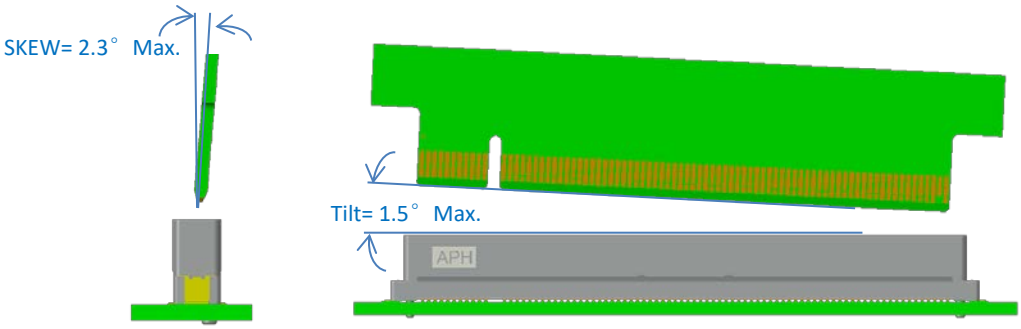
All signal pins(Gen 5): A=4.40mm ;B=2.60mm; Wipe length=A-B=1.80mm



Notes:

This is a generic calculation based on Amphenol Cool Edge tolerances and may be impacted by the PCB manufactures capabilities.

5.4 TILT AND SKEW

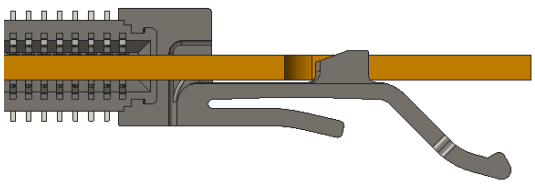


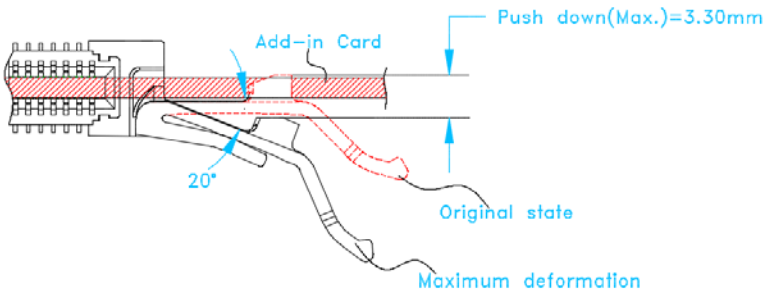
Notes:

This is a generic calculation based on Amphenol Cool Edge tolerances and may be impacted by the PCB manufactures capabilities.

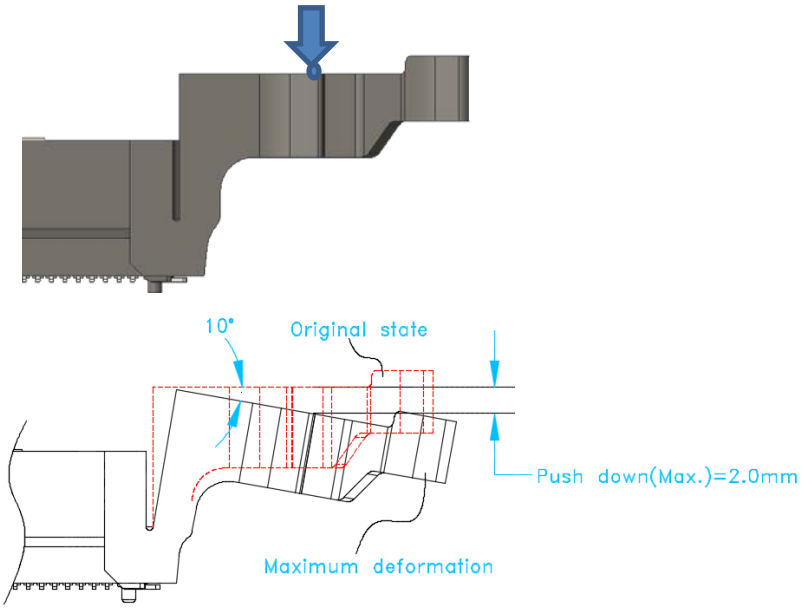
5.5 Latch deformation

Horizontal Load: Maximum deformation is 3.30mm or 20°

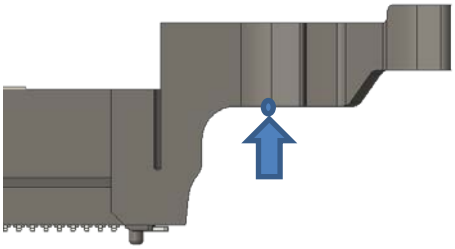




Vertical Load(1): Maximum deformation is 2.0mm or 10°

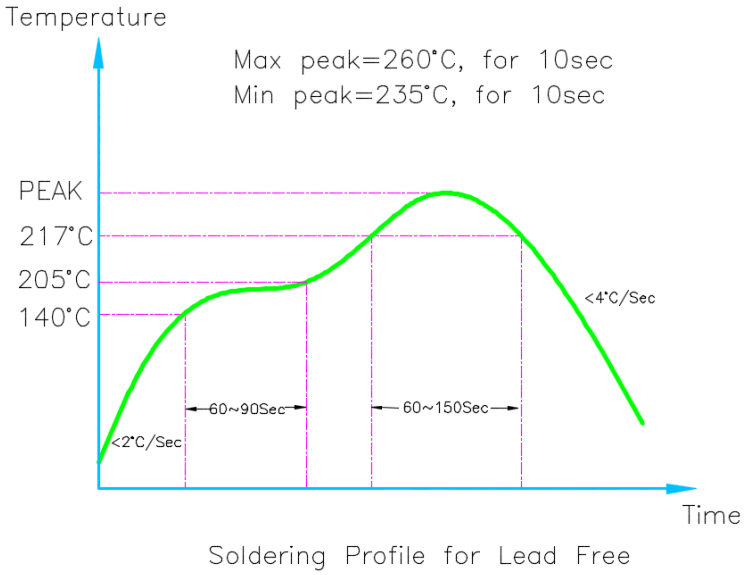


Vertical Load (2): allowable force on below direction is 50N Maximum.



6. RECOMMENDED REFLOW PROFILE

The recommended profile is below. Customers should develop parameters that best suit individual application requirements.



Soldering Profile for Lead Free

7. CONNECTOR PINOUT

7.1 TRAMISSION SPEED

PCIe GEN4/16Gbps: Open pin field design, that's mean do not have to connect all GND pin
PCIe GEN5/32Gbps: Conform to PCIe CEM specification, and all GND pins are connected by ECB component.

7.2 PCIe CEM INDUSTRIAL SPECIFICATION

For standard PCI Express application, the interface signal assignment as below (the definition is from PCIe CEM industrial standard).

Pin #	Side B Name	Side B Description	Side A Name	Side A Description
1	+12V	+12 V power	PRSNT1#	Hot Plug presence detect
2	+12V	+12 V power	+12V	+12 V power
3	+12V	+12 V power	+12V	+12 V power
4	GND	Ground	GND	Ground
5	SMBCLK	SMBus (System Management Bus) clock	JTAG2	TCK (Test Clock), clock input for JTAG interface
6	SMBDAT	SMBus (System Management Bus) Data	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	+3.3 V power	JTAG5	TMS (Test Mode Select)
9	JTAG1	TRST# (Test Reset) resets the JTAG interface	+3.3V	+3.3 V power
10	+3.3Vaux	+3.3 V auxiliary power	+3.3V	+3.3 V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental reset
Mechanical Key				
12	CLKREQ#	Clock Request Signal	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK-	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Hot Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
End of the x1 Connector				
19	PETp1	Transmitter differential pair, Lane 1	MFG	Manufacturer Test Mode
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, Lane 2	GND	Ground
24	PETn2		GND	Ground
25	GND	Ground	PERp2	Receiver differential pair, Lane 2
26	GND	Ground	PERn2	
27	PETp3	Transmitter differential pair, Lane 3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	PWRBRK#	Emergency Power Reduction	PERn3	
31	PRSNT2#	Hot Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
End of the x4 connector				
33	PETp4	Transmitter differential pair, Lane 4	RSVD	Reserved
34	PETn4		GND	Ground
35	GND	Ground	PERp4	Receiver differential pair, Lane 4
36	GND	Ground	PERn4	
37	PETp5	Transmitter differential pair, Lane 5	GND	Ground
38	PETn5		GND	Ground
39	GND	Ground	PERp5	Receiver differential pair, Lane 5
40	GND	Ground	PERn5	
41	PETp6	Transmitter differential pair, Lane 6	GND	Ground
42	PETn6		GND	Ground
43	GND	Ground	PERp6	Receiver differential pair, Lane 6
44	GND	Ground	PERn6	
45	PETp7	Transmitter differential pair, Lane 7	GND	Ground
46	PETn7		GND	Ground
47	GND	Ground	PERp7	Receiver differential pair, Lane 7
48	PRSNT2#	Hot Plug presence detect	PERn7	
49	GND	Ground	GND	Ground
End of the x8 Connector				
50	PETp8	Transmitter differential pair, Lane 8	RSVD	Reserved
51	PETn8		GND	Ground
52	GND	Ground	PERp8	Receiver differential pair, Lane 8
53	GND	Ground	PERn8	
54	PETp9	Transmitter differential pair, Lane 9	GND	Ground
55	PETn9		GND	Ground
56	GND	Ground	PERp9	Receiver differential pair, Lane 9
57	GND	Ground	PERn9	
58	PETp10	Transmitter differential pair, Lane 10	GND	Ground
59	PETn10		GND	Ground
60	GND	Ground	PERp10	Receiver differential pair, Lane 10
61	GND	Ground	PERn10	
62	PETp11	Transmitter differential pair, Lane 11	GND	Ground
63	PETn11		GND	Ground
64	GND	Ground	PERp11	Receiver differential pair, Lane 11
65	GND	Ground	PERn11	
66	PETp12	Transmitter differential pair, Lane 12	GND	Ground
67	PETn12		GND	Ground
68	GND	Ground	PERp12	Receiver differential pair, Lane 12
69	GND	Ground	PERn12	
70	PETp13	Transmitter differential pair, Lane 13	GND	Ground
71	PETn13		GND	Ground
72	GND	Ground	PERp13	Receiver differential pair, Lane 13
73	GND	Ground	PERn13	
74	PETp14	Transmitter differential pair, Lane 14	GND	Ground
75	PETn14		GND	Ground
76	GND	Ground	PERp14	Receiver differential pair, Lane 14
77	GND	Ground	PERn14	
78	PETp15	Transmitter differential pair, Lane 15	GND	Ground
79	PETn15		GND	Ground
80	GND	Ground	PERp15	Receiver differential pair, Lane 15
81	PRSNT2#	Hot Plug presence detect	PERn15	
82	RSVD	Reserved	GND	Ground
End of the x16 Connector				