Product Application Specification
Double Density Cool Edge Connector Vertical

REVISION RECORD

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1. OBJECTIVE

This specification provides information and requirements for customer application of the Double Density Cool Edge Vertical connector. It is intended to provide general guidance for process development. It should be recognized that no single process will work under all customer applications and the customers should develop processes to meet individual needs. However, if the processes vary from the recommended one, Amphenol cannot guarantee acceptable results.

2. SCOPE

This specification provides information and requirements regarding application of Double Density Cool Edge vertical connector to printed circuit boards (PCB). The connectors are designed for mother/daughter board applications and will accept different thickness of daughter card. They are available with multiple contact and power positions, latch and board lock are alternative.

Figure 1: Double Density Cool edge vertical connectors

3. DRAWING AND APPLICABLE DOCUMENTS

- Amphenol Product Specification S-CED-001
- Application Amphenol Customer Drawings

Amphenol product drawings and specifications are available by accessing the Amphenol website or contacting the Amphenol Technical Service. In the event of a conflict between this specification and the product drawing, the drawing takes precedence. Customers should refer to the latest revision level of Amphenol product drawings for appropriate product details.

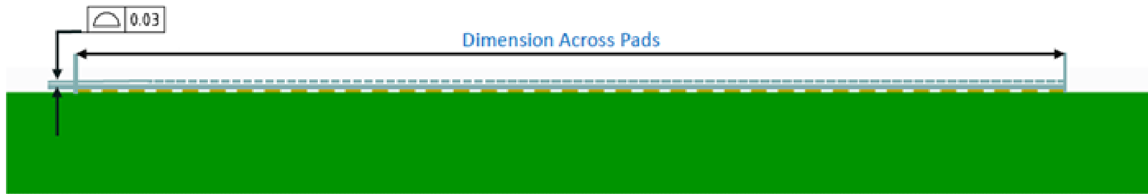
4. Printed Circuit Board (PCB) REQUIREMENTS

4.1 MATERIAL AND THICKNESS

The printed circuit board (PCB) material shall be glass epoxy (FR4 or G-10). The recommended minimum PCB (mother board) thickness shall be 1.57mm

4.2 PC BOARD (MOTHER BOARD) HIGH TEMPERATURE PAD CO-PLANARITY

Maximum allowable bow (co-planarity) shall be 0.03mm across the length of the pad area In the case of 0.13mm thick solder paste.



Maximum allowable bow (co-planarity) shall be 0.05mm across the length of the pad area In the case of 0.15mm thick solder paste.

4.3 STENCIL

The recommended stencil for the connector soldering to ensure placement on the mother board reliably. The recommended thickness, dimensions of hole for general and power application are provided in Figure 9 &10.

Figure 9: RECOMMENDED STENCIL THICKNESS REQUIRMENT
(YOUR CONFIGURATION MAY VARY)

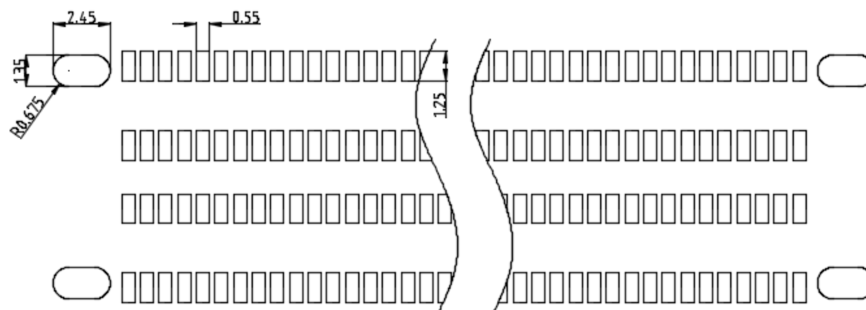


Figure 10: RECOMMENDED STENCIL FOR GENERAL
(YOUR CONFIGURATION MAY VARY)

4.4 PCB LAYOUT FOR SIGNAL

The holes for the connector assembly must be precisely located to ensure proper placement and optimum performance of the connector assembly. Recommended general holes, pads, dimensions, and tolerances are provided in Figure 2 to 5. It’s a general layout, please refer to appropriate sales drawing for recommended PCB layout and thickness for each parts.

FOR DD COOL EDGE CONNECTOR LESS THAN 148PIN ONLY

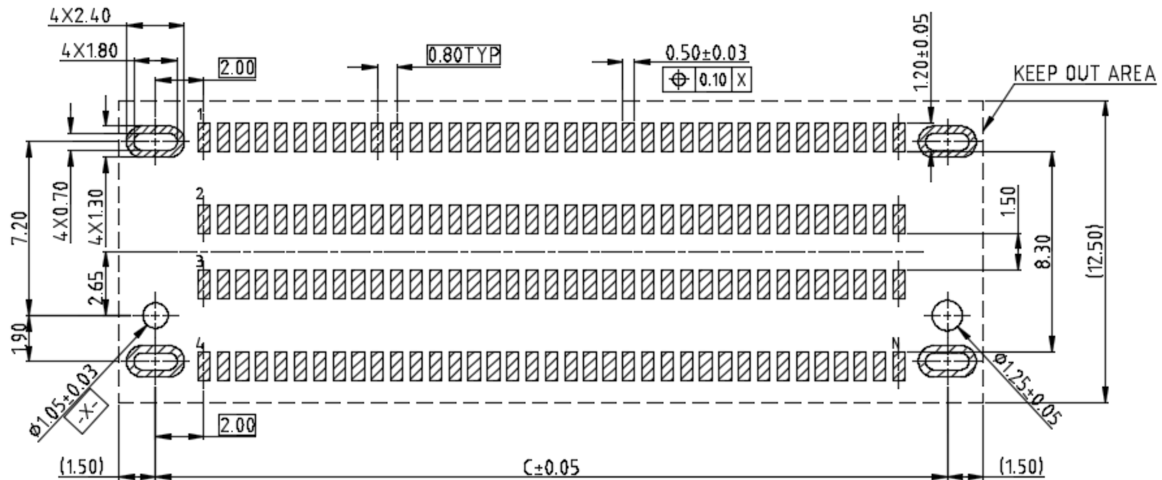


Figure 2: GENERAL PCB LAYOUT FOR MOTHER BOARD
(YOUR CONFIGURATION MAY VARY)

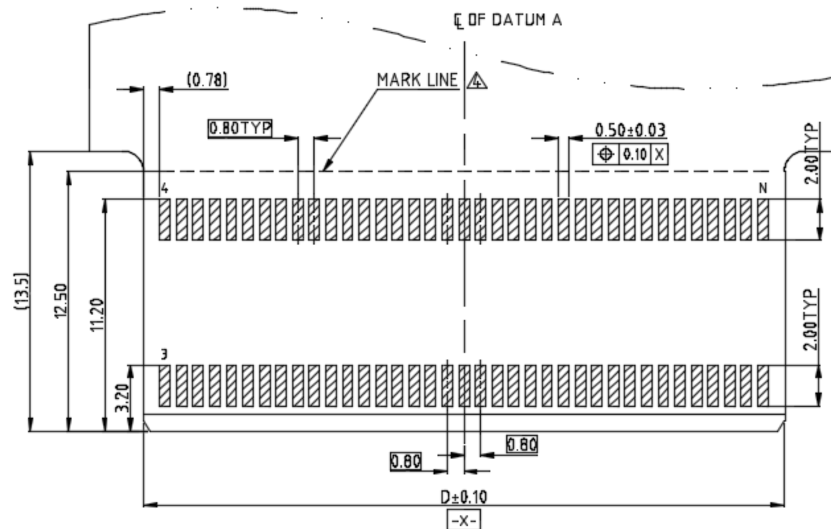


Figure 3: GENERAL PCB LAYOUT FOR AIC
(YOUR CONFIGURATION MAY VARY)

FOR DD COOL EDGE CONNECTOR MORE THAN 200PIN ONLY

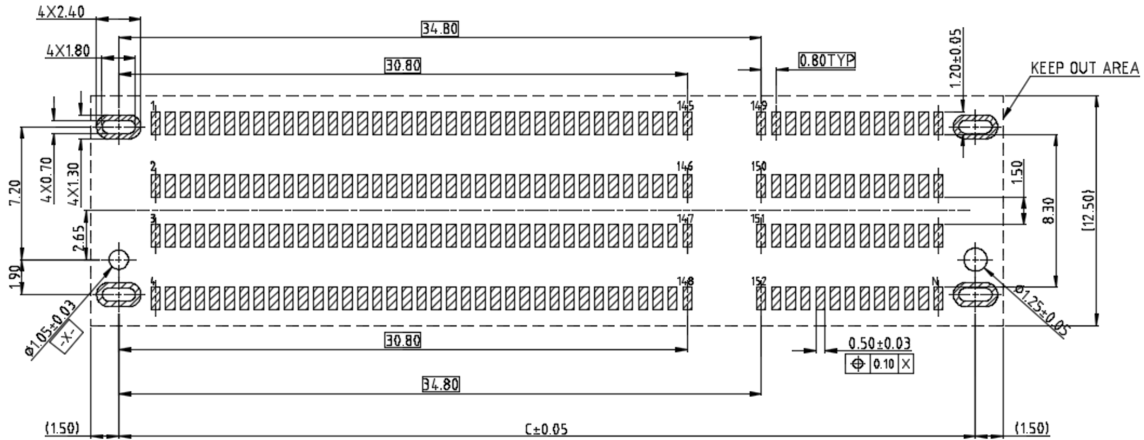


Figure 4: GENERAL PCB LAYOUT FOR MOTHER BOARD
(YOUR CONFIGURATION MAY VARY)

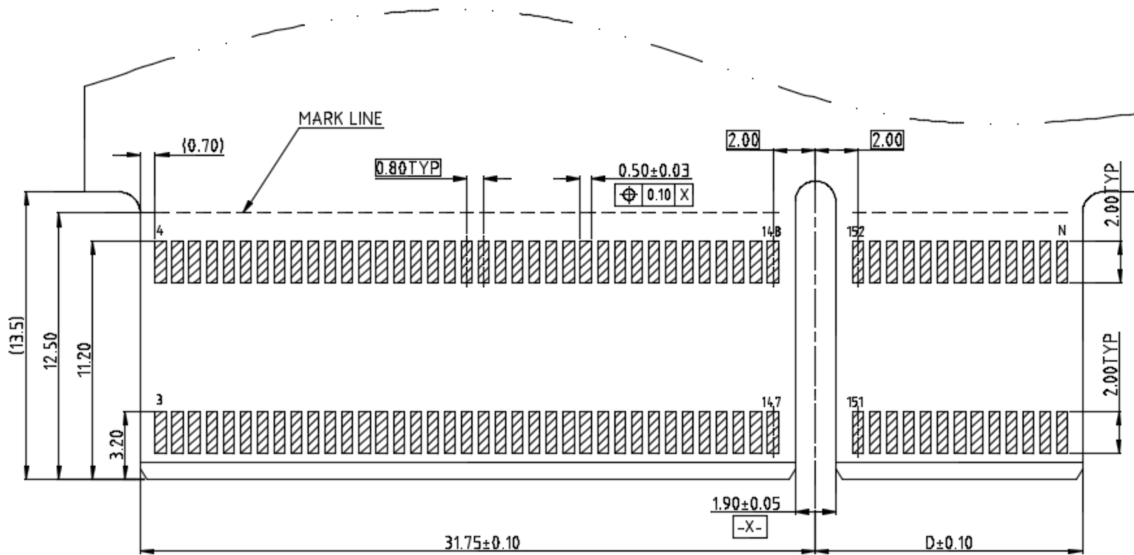


Figure 5: GENERAL PCB LAYOUT FOR AIC
(YOUR CONFIGURATION MAY VARY)

4.5 PCB LAYOUT FOR POWER APPLICATION

The holes for the connector assembly must be precisely located to ensure proper placement and optimum performance of the connector assembly. The recommended especial pads, dimension and PTH hole for power application base on 4.3 are provided in Figure 6&7, and layers with copper thickness requirement is provided in Figure 8.

FOR DD COOL EDGE CONNECTOR POWER APPLICATION

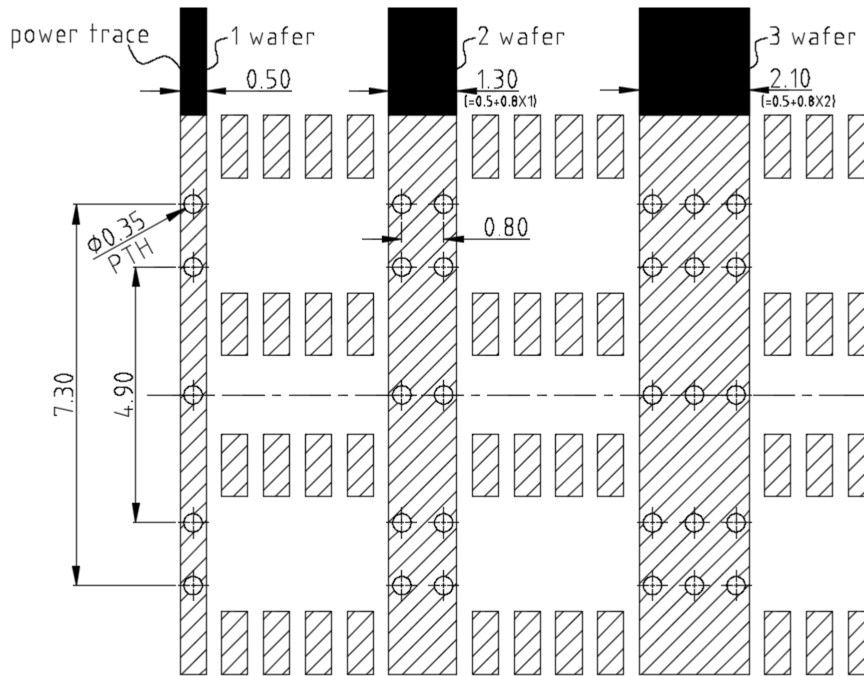


Figure 6: PCB LAYOUT FOR MOTHER BOARD WITH POWER
(YOUR CONFIGURATION MAY VARY)

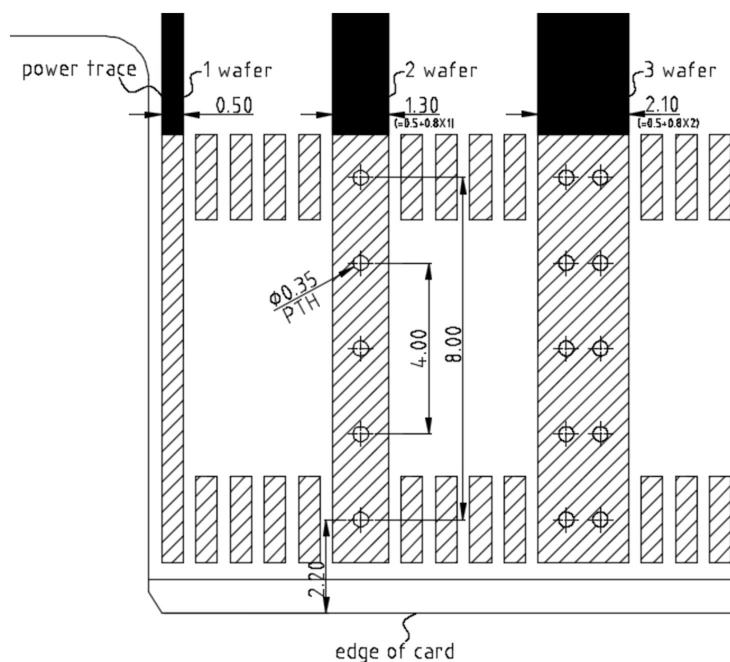


Figure 7: PCB LAYOUT FOR AIC WITH POWER
(YOUR CONFIGURATION MAY VARY)

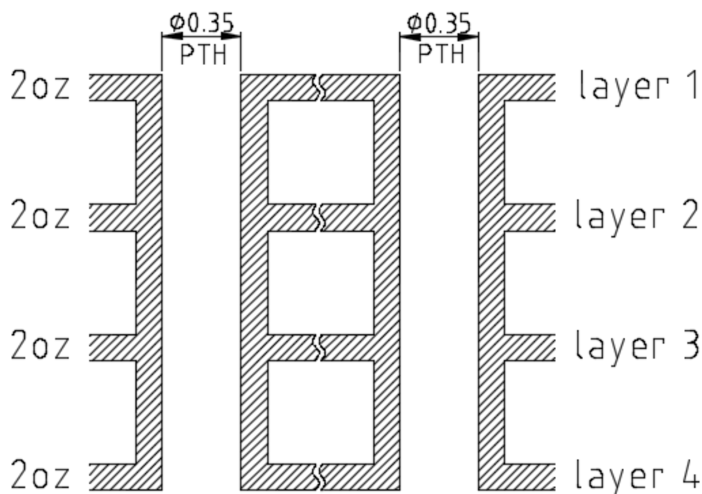


Figure 8: PCB LAYERS FOR MOTHER BOARD AND AIC WITH POWER
(YOUR CONFIGURATION MAY VARY)

5. CURRENT RATING FOR POWER WAFER AND SIGNAL WAFER.

Please refer to below table for current rating of power wafer (4 layer for PCB, 2oz copper for each layer)

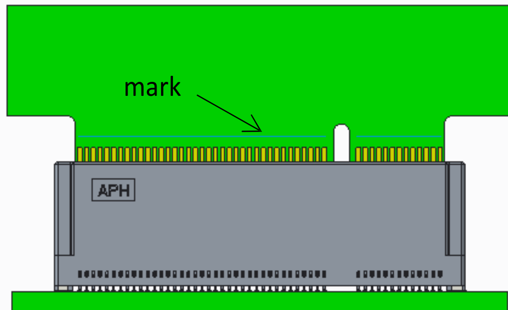
Wafer	Pin Qty	Current/pin (A)	Current/Wafer (A)	Total
1	4	2.375	9.5	9.5
2	8	2.06	8.25	16.5
3	12	1.75	7.0	21.0
4	16	1.56	6.25	25.0
5	20	1.4	5.6	28.0
6	24	1.29	5.16	31.0
7	28	1.25	5	35.0
8	32	1.18	4.75	38.0
9	36	1.138	4.55	41.0
10	40	1.075	4.3	43.0

Please refer to below table for current rating of Signal wafer (4 layer for PCB, 2oz copper for each layer)

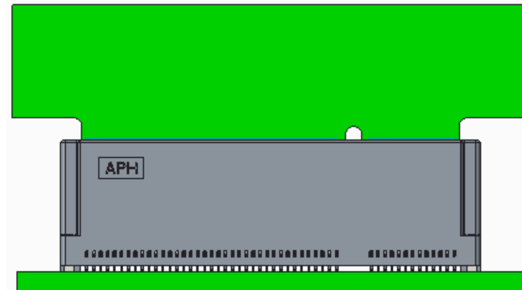
Wafer	Pin Qty	Current/pin (A)	Current/Wafer (A)	Total
1	4	1.0	4	4
2	8	0.975	3.9	7.8
3	12	0.933	3.73	11.2
4	16	0.8875	3.55	14.2
5	20	0.84	3.36	16.8
6	24	0.7875	3.15	18.9
7	28	0.725	2.9	20.3
8	32	0.675	2.7	21.6
9	36	0.6375	2.55	23.0
10	40	0.6075	2.43	24.3

6. MATING AND ALIGNMENT

6.1 TWO STAGES OF INSERTION



the first stage
(insert incompletely)



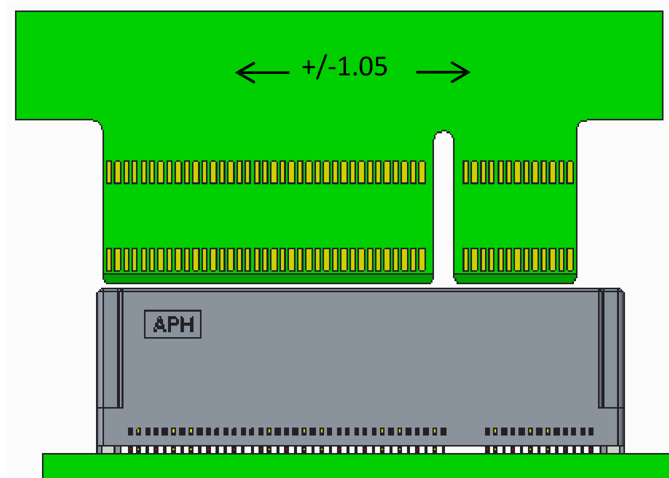
the second stage
(insert completely)

Notes:

1.mark a line (or other symbol) on the AIC to determine the it insert connector completely

6. 2 GUIDING FEATURES IN "X" DIRECTION

Nominal misalignment correction in "X" DIRECTION:+/-1.05mm



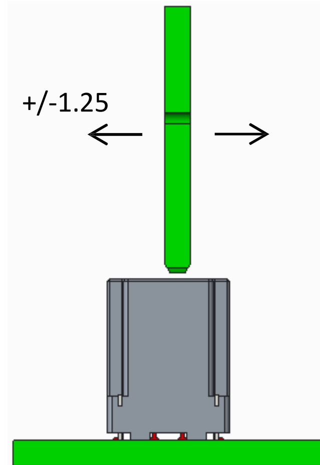
Misalignment in X direction

Notes:

1. This is a generic calculation based on Amphenol DD Cool Edge tolerances and may be impacted by the PCB manufactures capabilities.

6.3 GUIDING FEATURES IN "Y" DIRECTION, WITH GUIPDE PIN

Nominal misalignment correction in "Y" DIRECTION:+/-1.25mm

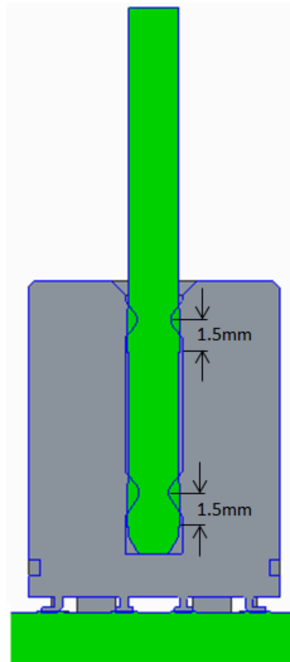


Misalignment in Y direction

Notes:

1. This is a generic calculation based on Amphenol DD Cool Edge tolerances and may be impacted by the PCB manufactures capabilities.

6.4 WIPE LENGTH

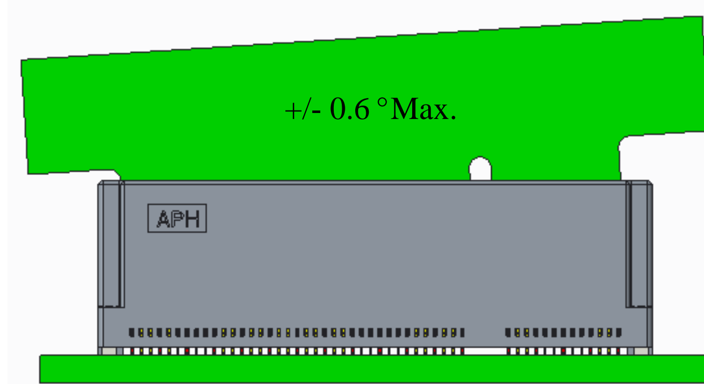


Wipe Length of upper and lower row

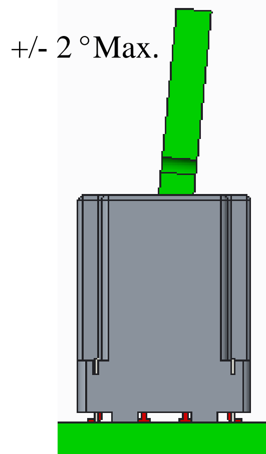
Notes:

1. This is a generic calculation based on Amphenol DD Cool Edge tolerances and may be impacted by the PCB manufactures capabilities.

6.5 TILT AND SKEW



ALLOWED THE MAX SKEW IN X DIRECTION

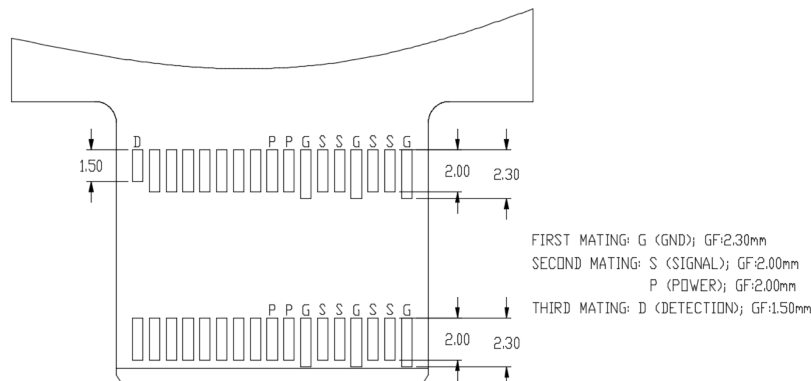


ALLOWED THE MAX SKEW IN Y DIRECTION

Notes:

1. This is a generic calculation based on Amphenol DD Cool Edge tolerances and may be impacted by the PCB manufactures capabilities.

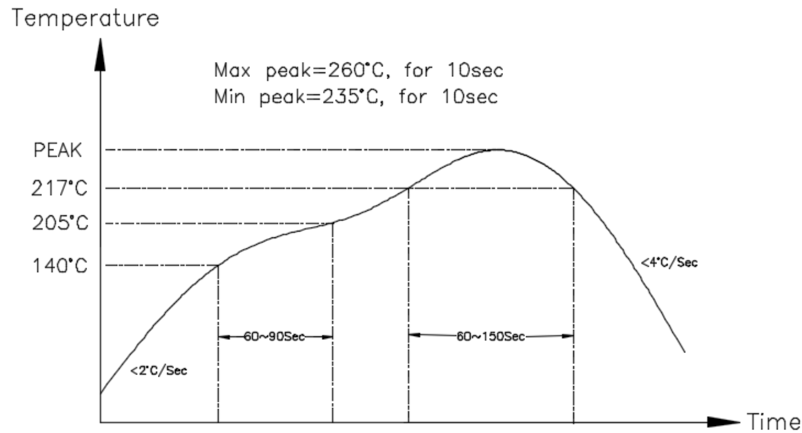
6.6 RECOMMENDED MATING SEQUENCE



Notes:

1. Recommended mating sequence for some special applications,

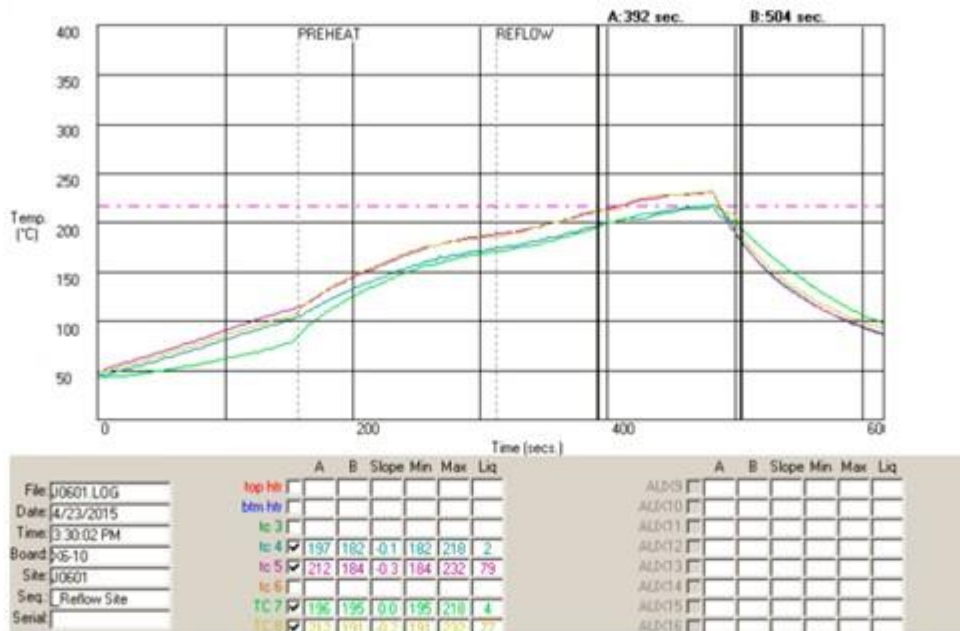
7. RECOMMENDED SOLDERING PROFILE FOR LEAD FREE



RECOMMENDED PROFILE FOR GENERAL
(YOUR CONFIGURATION MAY VARY)

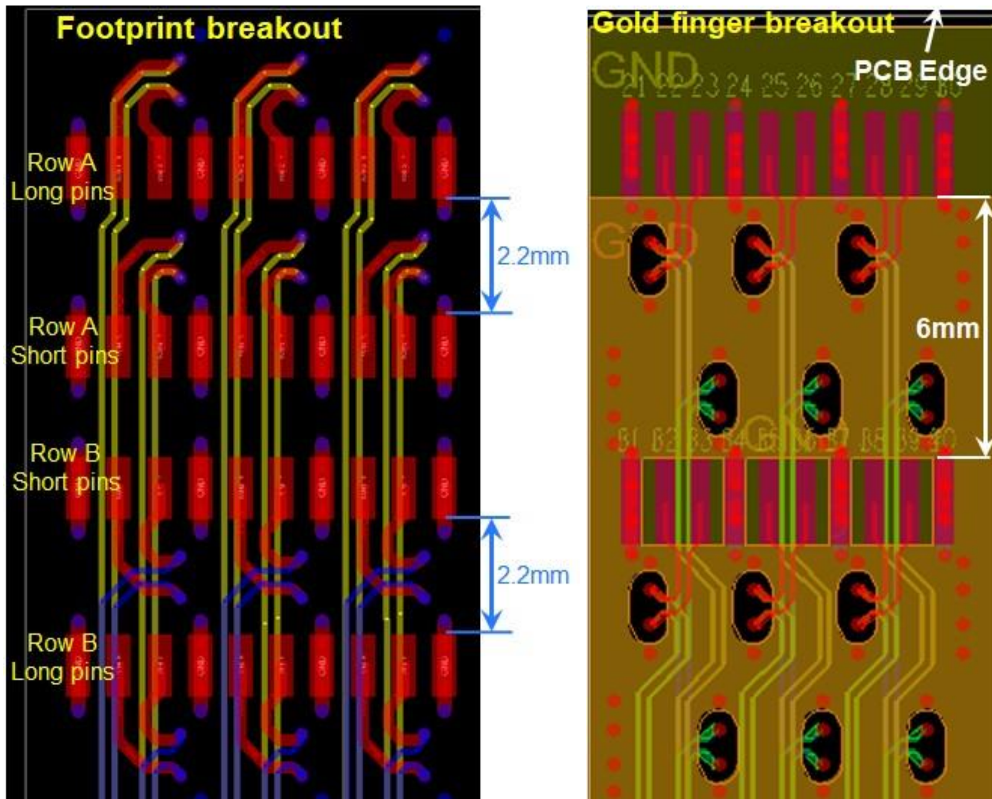
8. RECOMMENDED REWORK PROCESS

It can be reworked well under BGA rework station, and it needs to re-design and make mini-stencil to print those TH board lock together with SMT pads, it also needs to add a shield wall, it can avoid socket's housing material melting or bubble defect. The recommended rework profile is below.



9. RECOMMENDED BREAKOUT FOR SI.

The recommended breakout for the double density cool edge connector, it include PTH-via break out and micro via breakout.

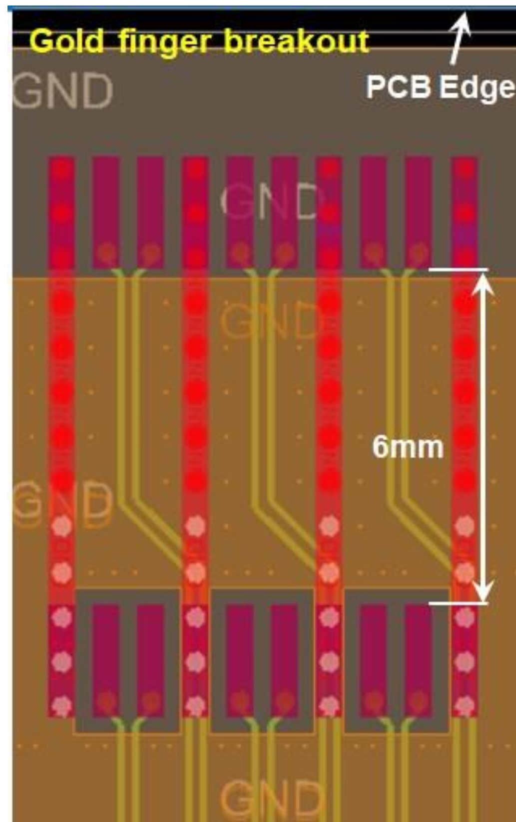


RECOMMENDED PTH-VIA BREAKOUT
(YOUR CONFIGURATION MAY VARY)

Notes:

1. Amphenol suggested AIC stackup as below (at least 10 layers), the more signal ground and power layer will be allowed to add.
2. Ground planes L2/9 voided out and L3/5/6/8 solid for AIC.
3. Top to L3 (or bottom to L8) thickness more than 0.3mm

	SURFACE
TOP	CONDUCTOR
	DIELECTRIC
L2 GND	PLANE
	DIELECTRIC
L3 GND	PLANE
	DIELECTRIC
L4 SIG	CONDUCTOR
	DIELECTRIC
L5 GND	PLANE
	DIELECTRIC
L6 GND	PLANE
	DIELECTRIC
L7 SIG	CONDUCTOR
	DIELECTRIC
L8 GND	PLANE
	DIELECTRIC
L9 GND	PLANE
	DIELECTRIC
BOTTOM	CONDUCTOR
	SURFACE



RECOMMENDED MICRO BREAKOUT FOR AIC
(YOUR CONFIGURATION MAY VARY)

Notes:

1. Amphenol suggested AIC stackup as below (at least 8 layers), the more signal ground and power layer will be allowed to add.
2. Ground planes L2/7 voided out underneath signal gold fingers and L4/5 solid for AIC.
3. Micro via from top to L3 for gold finger of top layers routing or bottom to L6 for Bottom layer gold finger routing.

	SURFACE
	DIELECTRIC
TOP	CONDUCTOR
	DIELECTRIC
L2 GND	PLANE
	DIELECTRIC
L3 SIG	CONDUCTOR
	DIELECTRIC
L4 GND	PLANE
	DIELECTRIC
L5 GND	PLANE
	DIELECTRIC
L6 SIG	CONDUCTOR
	DIELECTRIC
L7 GND	PLANE
	DIELECTRIC
BOTTOM	CONDUCTOR
	DIELECTRIC
	SURFACE