TB-2149

XCede® Product Family Routing Guidelines

Revision "Y"

Specification Revision Status

Revision	SCR No.	Description	Initial	Date
R	S4446	Changed document title, added X2 routing, and Femto compliant pin	B. Merrill	3-30-16
T	S5051	Section 5.7 : Minimum critical working zone 0.75mm was 0.70mm on Femto compliant	B. Merrill	10-27-16
U	S5335	Figure 11; added Femto dual diameter via.	B. Merrill	1-16-17
V	S7211	Figure 8; 1.1mm was 1.0mm.	T. Nierendorf	10-9-18
W	S7703	Section 5.10.2; "Resulting ground plane…" 0.0044 was 0.003	T. Nierendorf	5-22-19
Y	S9658	Added section 4.2.7	D Smith	3-1-2022

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1. Scope

1.1 Intent

The intent of this technical bulletin is to outline the standard signal trace widths, minimum spacing requirements, and finish hole size requirements for XCede® product family interconnect systems when used in differential signal applications and low speed applications. The XCede product family encompasses XCede®, XCede Plus®, and X2 product lines, and their corresponding product derivatives including; Daughtercard, backplane, mezzanine, right-angle-male (RAM), orthogonal, right-angle-male direct-attach orthogonal (RAM DA ortho), and cable backplane interconnect systems. This document supersedes all other XCede® product family documents including customer use drawings when conflicts exist for the stated requirements outlined within this document. Unless stated or implied otherwise, “XCede” refers to any product or derivative within the XCede product family.

1.2 Efficient routing

Efficient routing of signal traces between connector patterns improves yields and manufacturability. Spacing between trace/pad and trace/trace needs to be considered to allow for proper feature modifications needed for the inner layer fabrication process. Failure to allow for this may result in lower yields and higher PWB costs.

1.3 Finished Hole Sizes

All finished hole size requirements provided within this document are based on testing completed in FR-4 laminate.

2. Definitions

2.1 Fillets

An extension of the pad at the interface of the trace to the pad that will allow more pad area, in the event that the pad to hole registration compromises the interconnect area. See Figure for details. For further information regarding these routing guidelines, please contact ATCS Applications Engineering.

2.2 Foils/Copper Weights

Copper foil is measured in ounces (or weight). Common copper weights are 0.5 ounces, 1 ounce, 1.5 ounces and 2 ounces (3 ounces up to 10 ounces are available for special order). 1 ounce = 0.0014”, 1.5 ounces = 0.0021”, 2 ounces = 0.0028”.

2.3 Pads/Lands/Annular Ring

A pad is the support around a hole. If you see a specification calling out an annular ring of 0.005”, that will mean the amount of the pad left around the hole after processing.

2.4 Spacing

Spacing is the space between two electrical connections; it can be between two lines, two pads, a line and a pad etc.

2.5 Trace/Circuit/Line Width/Lines/Conductor

These are different terms for a connection. If you see the term 0.008” lines, it means the electrical connection from one point to another will measure 0.008” width.

2.6 Backplane
When used within this document refers to the PCB associated with the male connector half of the connector system mounted to a fixed PCB in a chassis.

2.7 Daughtercard
When used within this document refers to the PCB associated with the female connector half of the connector system mounted to a plug-in card in a chassis.

3. Routing Guidelines

3.1 Minimum Spacing
Minimum spacing, specific pad/trace, and trace/trace between all features should be 0.005” (.127mm) to allow for manufacturing tolerances.

3.2 Impedance
Consider characteristic impedance (if applicable) when designing to ensure line widths will meet requirements. Please contact ATCS Application Engineering for impedance calculations.

3.3 Copper Weights
Consider copper weights when routing. Higher weights will impact minimum trace widths.

3.4 Fillets
Fillets at the interface (egress) of the trace to the pad are required to improve annular ring when the electrical design requires tight hole to pad configurations.

3.5 Trace Centering
Center all traces between holes to optimize spacing.

3.6 Non Functional Pads
For high speed applications, remove all non-functional pads.

4. Design Rules and Manufacturability Guidelines

4.1 General Design Rules

4.1.1 XCede® Drill
Short Tail Hole: ISO 0.45mm (0.0177”)
Medium Tail Hole: ISO 0.55mm (0.0217”).
Long Tail Hole: ISO 0.57mm (0.0225”) drill (#74)

4.1.2 XCede® Plus Drill
Short Tail Hole: ISO 0.45mm (0.0177”)

4.1.3 XCede® X2 Drill
Femto Tail Hole: ISO 0.40mm (0.0157”)

4.1.4 Footprint
For specific connector footprint see customer use drawings.

4.1.5 Drilled Hole and Copper Thickness

For copper wall thickness requirements and finish hole size reference, see Table 5 and Table 6.

4.2 Daughtercard/Backplane Manufacturability Guidelines

4.2.1 Line Widths, Pad Sizes and Spacing

Line widths, pad sizes and spacing applicable for 1/2 ounce and 1 ounce copper weights.

4.2.2 Filleting

Filleting of pads recommended (to be added by fabricator) for 0.000” annular ring (tangency), see Figure .

4.2.3 Minimum PCB Thickness

Long Tail: Recommended minimum pcb thickness of 0.063” (1.60mm).
Medium, Short and Femto Tail: Recommended minimum pcb thickness of 0.043” (1.1 mm).

4.2.4 Non-functional pads

Non-functional pads on signal can be removed at designer’s option.

4.2.5 Plane Clearances

Plane clearances are applicable for copper weights up to 2 ounces. Please contact ATCS Application Engineering for applications with more than 2 ounce copper.

4.2.6 Surface Traces

Surface traces are not recommended. If surface traces are used refer to the customer drawings for keep-out zones.

4.2.7 Conductive Surface Layer (X2 connectors only)

It is required that the top surface layer which the X2 connector is pressed into has a conductive ground layer free from insulating coating (soldermask) in the connector footprint region. The surface ground plane is to equal the component outline.

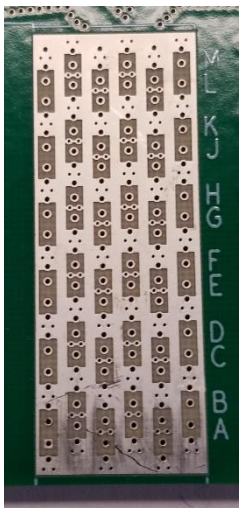

Figure 1

5. Routing Guidelines

Short tail compliant pins are used on the high-speed differential signal backplane headers and the stacker modules.

5.1 XCede® and XCede® Plus Short Tail Signal Pad Sizes

PCB Material Thickness, in (mm)	Copper Weight Ounces	Process	Min. Pad Size 0.000 A/R, in (mm)	Min. Pad Size 0.001 A/R, in (mm)	Min. Pad Size 0.002 A/R, in (mm)
0.035 to 0.400 (1.1 to 10.16)	0.5 (17μm)	Inner Layer	0.03 (0.76)	0.032 (0.81)	0.034 (0.86)
		Outer Layer	0.032 (0.81)	0.034 (0.86)	0.036 (0.91)
0.035 to 0.400 (1.1 to 10.16)	1.0 (35μm)	Inner Layer	0.031 (0.79)	0.033 (0.84)	0.035 (0.89)
		Outer Layer	0.033 (0.84)	0.035 (0.89)	0.037 (0.94)
0.035 to 0.400 (1.1 to 10.16)	2.0 (70μm)	Inner Layer	0.033 (0.84)	0.035 (0.89)	0.037 (0.94)
		Outer Layer	0.035 (0.86)	0.037 (0.91)	0.039 (0.99)

Table 1: XCede® and XCede® Plus Short Tail Minimum Pad Size vs. Copper Weight and Annular Ring ("A/R")

Notes for Table 1:

1. Outer layer pad sizes reflect panel plating process.
2. Use inner layer pad sizes for outers when pattern plating.
3. Values in ( ) are metric equivalents. For printed circuit board layout use metric units.

5.2 X2 Femto Tail Signal Pad Sizes

PCB Material Thickness, in (mm)	Copper Weight Ounces	Process	Min. Pad Size 0.000 A/R, in (mm)	Min. Pad Size 0.001 A/R, in (mm)	Min. Pad Size 0.002 A/R, in (mm)
0.035 to 0.400 (1.1 to 10.16)	0.5 (17μm)	Inner Layer	0.026 (0.66)	0.028 (0.71)	0.030 (0.76)
		Outer Layer	0.028 (0.71)	0.030 (0.76)	0.032 (0.81)
0.035 to 0.400 (1.1 to 10.16)	1.0 (35μm)	Inner Layer	0.027 (0.79)	0.029 (0.74)	0.031 (0.79)
		Outer Layer	0.029 (0.68)	0.031 (0.79)	0.033 (0.84)
0.035 to 0.400 (1.1 to 10.16)	2.0 (70μm)	Inner Layer	0.029 (0.68)	0.031 (0.79)	0.034 (0.86)
		Outer Layer	0.031 (0.79)	0.033 (0.84)	0.035 (0.89)

Table 2: X2 Femto Tail Minimum Pad Size vs. Copper Weight and Annular Ring ("A/R")

Notes for Table 2:

1. Outer layer pad sizes reflect panel plating process.

2. Use inner layer pad sizes for outers when pattern plating.
3. Values in ( ) are metric equivalents. For printed circuit board layout use metric units.
4.

5.3 XCede® Medium Tail Signal Pad Sizes

PCB Material Thickness, in (mm)	Copper Weight Ounces	Process	Min. Pad Size 0.000 A/R, in (mm)	Min. Pad Size 0.001 A/R, in (mm)	Min. Pad Size 0.002 A/R, in (mm)
0.062 to 0.400 (1.57 to 10.2)	0.5 (17μm)	Inner Layer	0.034 (0.86)	0.036 (0.91)	0.038 (0.97)
		Outer Layer	0.036 (0.91)	0.038 (0.97)	0.040 (1.02)
0.062 to 0.400 (1.57 to 10.2)	1.0 (35μm)	Inner Layer	0.035 (0.89)	0.037 (0.94)	0.039 (1.00)
		Outer Layer	0.037 (0.94)	0.039 (0.99)	0.041 (1.04)
0.062 to 0.400 (1.57 to 10.2)	2.0 (70μm)	Inner Layer	0.037 (0.94)	0.039 (0.99)	0.041 (1.04)
		Outer Layer	0.039 (0.99)	0.041 (1.04)	0.043 (1.09)

Table 3: XCede® Medium Tail Minimum Pad Size vs. Copper Weight and Annular Ring ("A/R")

Notes for Table 3:
1. Outer layer pad sizes reflect panel plating process.
2. Use inner layer pad sizes for outers when pattern plating.
3. Values in ( ) are metric equivalents. For printed circuit board layout use metric units.

5.4 XCede® Long Tail Signal Pad Sizes (see also Appendix B)

PCB Material Thickness, in (mm)	Copper Weight Ounces	Process	Min. Pad Size 0.000 A/R, in (mm)	Min. Pad Size 0.001 A/R, in (mm)	Min. Pad Size 0.002 A/R, in (mm)
0.062 to 0.400 (1.57 to 10.2)	0.5 (17μm)	Inner Layer	0.035 (0.89)	0.037 (0.94)	0.039 (0.99)
		Outer Layer	0.037 (0.94)	0.039 (0.99)	0.041 (1.04)
0.062 to 0.400 (1.57 to 10.2)	1.0 (35μm)	Inner Layer	0.036 (0.91)	0.038 (0.97)	0.040 (1.02)
		Outer Layer	0.038 (0.97)	0.040 (1.02)	0.042 (1.07)
0.062 to 0.400 (1.57 to 10.2)	2.0 (70μm)	Inner Layer	0.038 (0.97)	0.040 (1.02)	0.042 (1.07)
		Outer Layer	0.040 (1.02)	0.042 (1.07)	0.044 (1.12)

Table 4: XCede® Long Tail Minimum Pad Size vs. Copper Weight and Annular Ring ("A/R")

Notes for Table 4:
1. Outer layer pad sizes reflect panel plating process.
2. Use inner layer pad sizes for outers when pattern plating.

3. Values in ( ) are metric equivalents. For printed circuit board layout use metric units.

5.5 Copper Thickness Requirement and Finished Thickness Reference

Finish Type	Copper thickness, in (mm) per side	Drill size, in (mm)	Typical Finish Thickness	Finished Hole Size, in (mm)
Lead Free HASL	0.0010 (0.0254) min 0.0025 (0.0635) max	Long Tail: 0.0225 (0.57) Medium Tail: 0.0225 (0.57)	500 micro inches maximum	0.019 +0.0015/-0.002(0.48+0.0381/-0.05)
Solder Finish (1)	0.0010 (0.0254) min 0.0025 (0.0635) max 0.0008 (0.020) min Short tail 0.00275 (0.069) max Short tail 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	Long Tail: 0.0225 (0.57) Medium Tail: 0.0217 (0.55) Short Tail: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	300 to 500 micro inches	Long Tail: 0.018 +/- 0.002 (0.46 +/- 0.05) Medium Tail: 0.0177 +/- 0.002 (0.45 +/- 0.05) Short Tail: 0.0142+/- 0.002 (0.36+/-0.05) Femto Tail: 0.0122+/- 0.002 (0.31+/-0.05)
Immersion Sn (Tin)	0.0010 (0.0254) min 0.0025 (0.0635) max 0.0008 (0.020) min Short tail 0.00275 (0.069) max Short tail 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	Long Tail: 0.0225 (0.57) Medium Tail: 0.0217 (0.55) Short Tail: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	35 to 75 micro inches minimum	Long Tail: 0.018 +/- 0.002 (0.46 +/- 0.05) Medium Tail: 0.0177 +/- 0.002 (0.45 +/- 0.05) Short Tail: 0.0142+/- 0.002 (0.36+/-0.05) Femto Tail: 0.0122+/- 0.002 (0.31+/-0.05)
Immersion Ag (Silver)	0.0010 (0.0254) min 0.0025 (0.0635) max 0.0008 (0.020) min Short tail 0.00275 (0.069) max Short tail 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	Long Tail: 0.0225 (0.57) Medium Tail: 0.0217 (0.55) Short Tail: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	4 micro inches minimum	Long Tail: 0.018 +/- 0.002 (0.46 +/- 0.05) Medium Tail: 0.0177 +/- 0.002 (0.45 +/- 0.05) Short Tail BP: 0.0142 +/- 0.002 (0.36+/-0.05) Short Tail DC: 0.0142 +0.002/-0.001 (0.36+0.05/-0.025) Short Tail DC: 0.0142 +0.002/-0.001 (0.36+0.05/-0.025) Femto Tail DC: 0.0122 +0.002/-0.001 (0.31+0.05/-0.025)
Copper - OSP	0.0010 (0.0254) min 0.0025 (0.0635) max (DC) 0.0030 (0.0762) max (BP) 0.0008 (0.020) min Short tail 0.00275 (0.069) max Short tail 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	Long Tail: 0.0225 (0.57) Medium Tail: 0.0217 (0.55) Short Tail: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	N/A	Long Tail: 0.018 +/- 0.002 (0.46 +/- 0.05) Medium Tail: 0.0177 +/- 0.002 (0.45 +/- 0.05) Short Tail: 0.0142+/- 0.002 (0.36+/-0.05) FemtoTail: 0.0122+/- 0.002 (0.31+/-0.05)
Ni Au (Nickel-Gold)	0.0010 (0.0254) min 0.0025 (0.0635) max 0.0008 (0.020) min Short tail 0.00275 (0.069) max Short tail 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	Long Tail: 0.0225 (0.57) Medium Tail: 0.0217 (0.55) Short Tail: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	53 to 210 micro inches Ni-Au compositions combined	Long Tail: 0.018 +/- 0.002 (0.46 +/- 0.05) Medium Tail: 0.0177 +/- 0.002 (0.45 +/- 0.05) Short Tail BP: 0.0142+/- 0.002 (0.36+/-0.05) Short Tail DC: 0.0142+/- 0.002 (0.36+/-0.05) Femto Tail BP: 0.0122+/- 0.002 (0.31+/-0.05) Femto Tail DC: 0.0122+/- 0.002 (0.31+/-0.05)

Table 5: Copper Thickness Requirement and Finished Thickness Reference

Finish Type	Copper thickness, in (mm) per side	Drill size, in (mm)	Typical Finish Thickness	Finished Hole Size, in (mm)
Solder Finish (1)	0.0008 (0.020) min Short tail 0.00275 (0.069) max Short tail	Short Tail: 0.0189 (0.48)	300 to 500 micro inches	Short Tail: 0.0154+/- 0.002 (0.39+/-0.05)
Immersion Sn (Tin)	0.0008 (0.020) min Short tail 0.00275 (0.069) max Short tail	Short Tail: 0.0189 (0.48)	35 to 75 micro inches minimum	Short Tail: 0.0154+/- 0.002 (0.39+/-0.05)
Immersion Ag (Silver)	0.0008 (0.020) min Short tail 0.00275 (0.069) max Short tail	Short Tail: 0.0189 (0.48)	4 micro inches minimum	Short Tail: 0.0154+/- 0.002 (0.39+/-0.05)
Copper - OSP	0.0008 (0.020) min Short tail 0.00275 (0.069) max Short tail	Short Tail: 0.0189 (0.48)	N/A	Short Tail: 0.0154+/- 0.002 (0.39+/-0.05)
Ni Au (Nickel-Gold)	0.0008 (0.020) min Short tail 0.00275 (0.069) max Short tail	Short Tail: 0.0189 (0.48)	53 to 210 micro inches Ni-Au compositions combined	Short Tail: 0.0154+/- 0.002 (0.39+/-0.05)

Table 6: Copper Thickness Requirement and Finished Thickness Reference. For use with 0.0189" drill for BP connector applications only (See Note 6).

NOTES (table 5 and 6):

1. Solder finish includes: Tin/lead reflowed (plated and reflowed) and HASL. Cu and HASL finished must combine to achieve the finished hole size specified.

Copper thickness per side is an Amphenol requirement. The copper plating must be within specified range in Table 5: Copper Thickness Requirement and Finished Thickness Reference

according to the specific Finish Type selected by the end user. Copper plating at the knee of the hole is limited to a maximum of 10% above the average copper wall thickness measured in the working zone, see Figure below, of the plated thru hole, and cannot exceed the MAX copper plating thickness specified in Table 5: Copper Thickness Requirement and Finished Thickness Reference

2. .

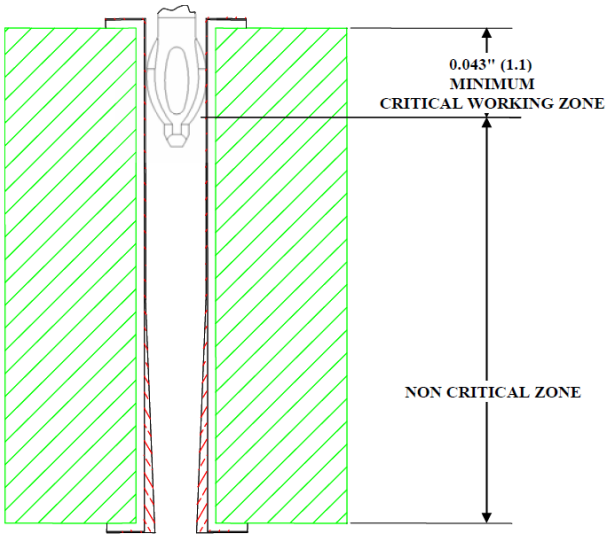

Figure 2: Nano Compliant Working Zone

3. Drill size is an Amphenol requirement. Amphenol requires this drill to be used as outlined in table 5. The drill size specified does not include a tolerance nor does it include a drilled hole tolerance. These tolerance allowances are included in the overall tolerance outlined in the Finish Hole Size tolerance reference range.
4. Typical Finish Thickness is an Amphenol reference value. Amphenol highlights the reference values on these finishes as a guideline for processing and inspection of PCB holes. Actual finish thicknesses will vary depending on the finish type selected by the end used design guidelines. However for ENIG, the nickel plating thickness is not a reference but is a requirement.
5. Finish Hole Size is an Amphenol Nominal Value. The Finish Hole Size tolerance for each finish type accounts for the accumulation of tolerances in the actual Drill Hole Diameter as a result of using the specified drill noted in the table above and Finish Thickness over the range of holes in a connector-hole pattern on a PCB. Cu thickness, finish plating thickness, and Drill Size must be adhered to per Amphenol's requirements in this document, but not cumulatively exceeded where these tolerance buildups exceed the finish hole requirements called out.
6. (Table 6 only). Consult ATCS Engineering for guidelines when selecting the 0.0189” drill in place of the 0.0177” drill for Backplane (vertical headers) only. In certain instances where there are high aspect drill ratios due to PCB thickness (i.e. greater than 0.250” > 14/1 ratios), achieving minimum plating thicknesses in the center of the PTH barrel can force the PTH mean to be at the low end of the FHS range and cause lower press yields. Using a drill of 0.0189” will shift the mean of the PTH 0.0014” higher.

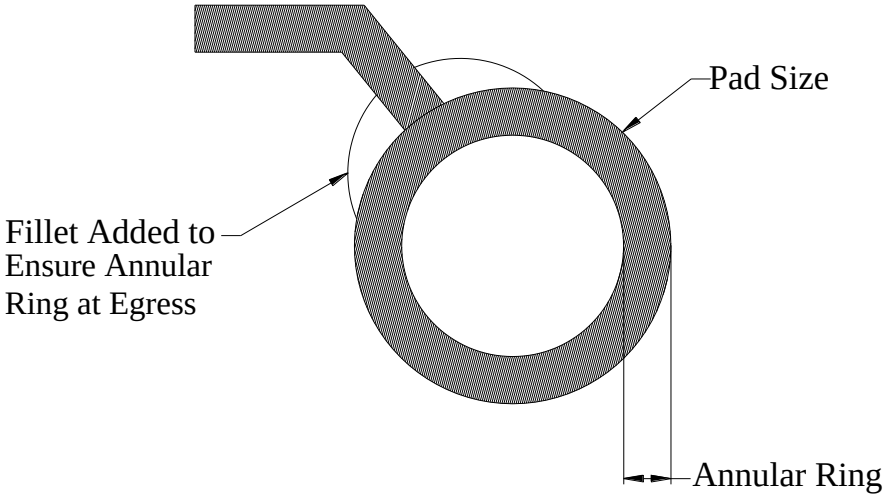

Figure 3: Preferred Fillet

Fillet Diameter equals one half size of plated through hole pad diameter located on a line central to trace so that fillet size equals minimum annular ring plus 0.005 (0.13).

5.6 Drill and Finished Hole Size

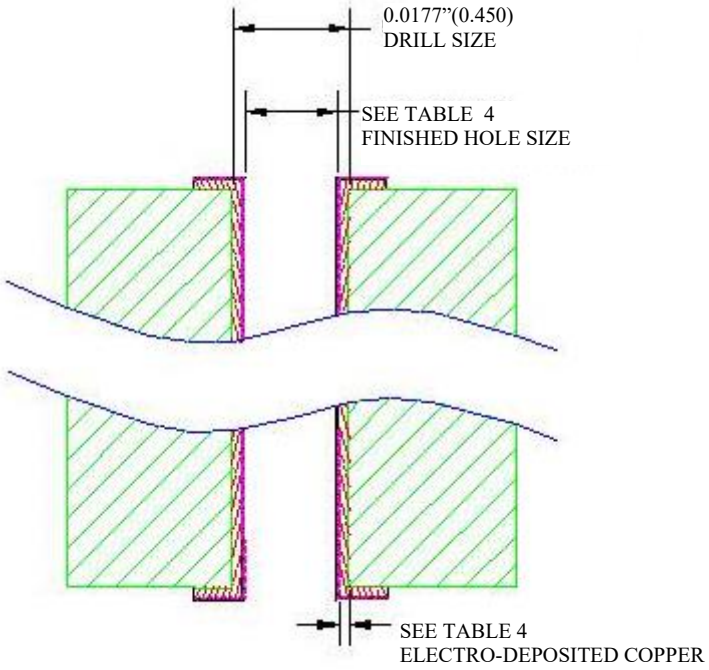

Figure 4: XCede® and XCede® Plus Short Tail (0.0177”) Drill and Finished Hole Size

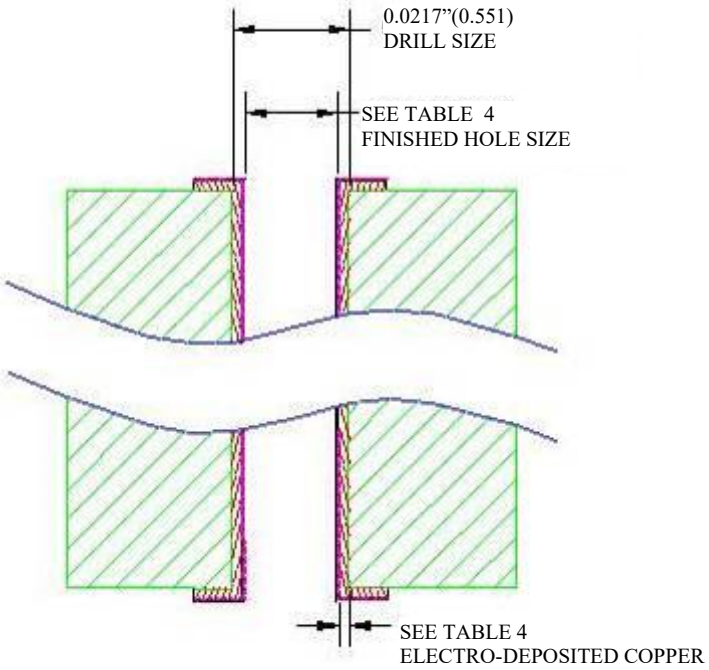

Figure 5: XCede® Medium Tail Drill (0.0217”) and Finished Hole Size

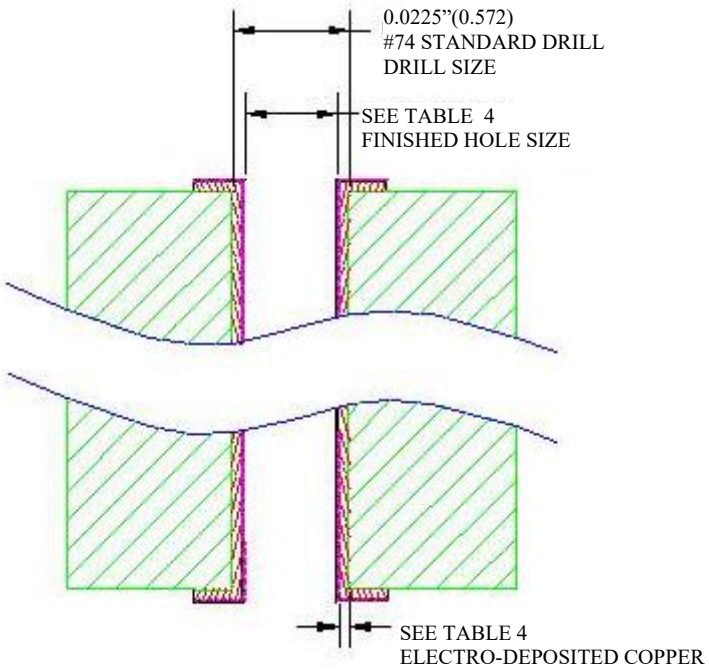

Figure 6: XCede® Long Tail Drill (0.0225”) and Finished Hole Size

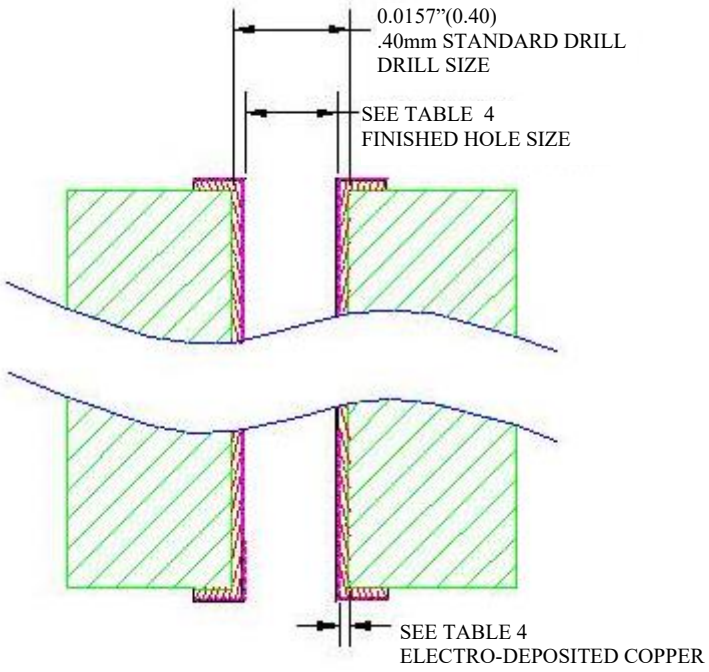

Figure 7: XCede® Femto Tail Drill (0.0157”) and Finished Hole Size

5.7 Compliant Pin Critical Zone

The “Critical Working Zone” shown in the following figures is defined as the compliant working zone where the plated through hole requirements must meet the specifications defined within this document. In the “Non Critical Zone”, the plated through hole is allowed to go below the minimum required finish hole size for non-midplane applications. Back drilling is allowed in the “non-critical zone” only.

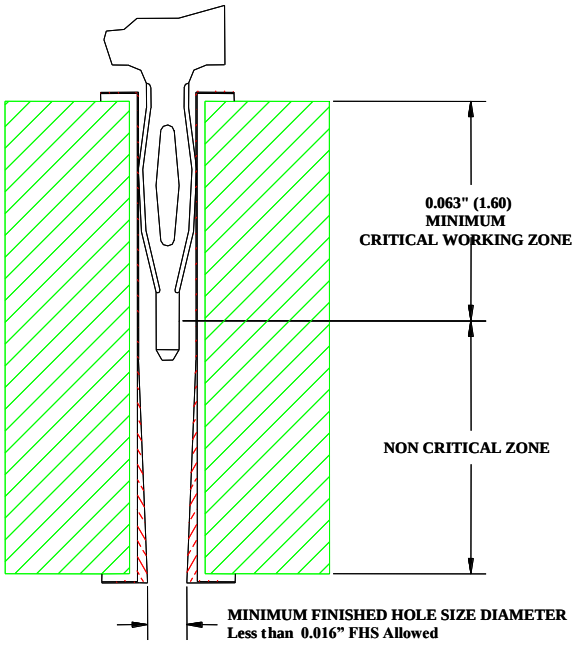

Figure 8: XCede® Long Tail (0.0225”) Compliant Pin Critical Zone

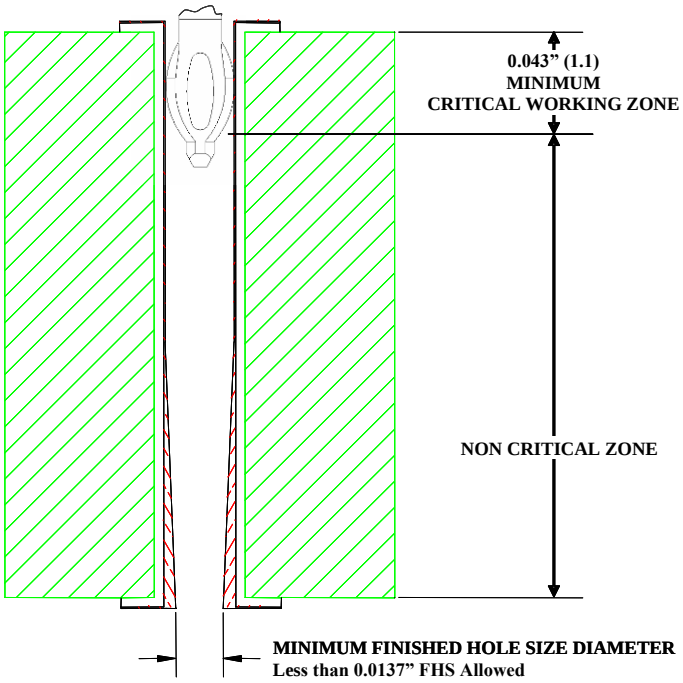

Figure 9: XCede® Medium (0.0217”) and Short Tail (0.0177”) and XCede® Plus Short Tail Compliant Pin Critical Zone

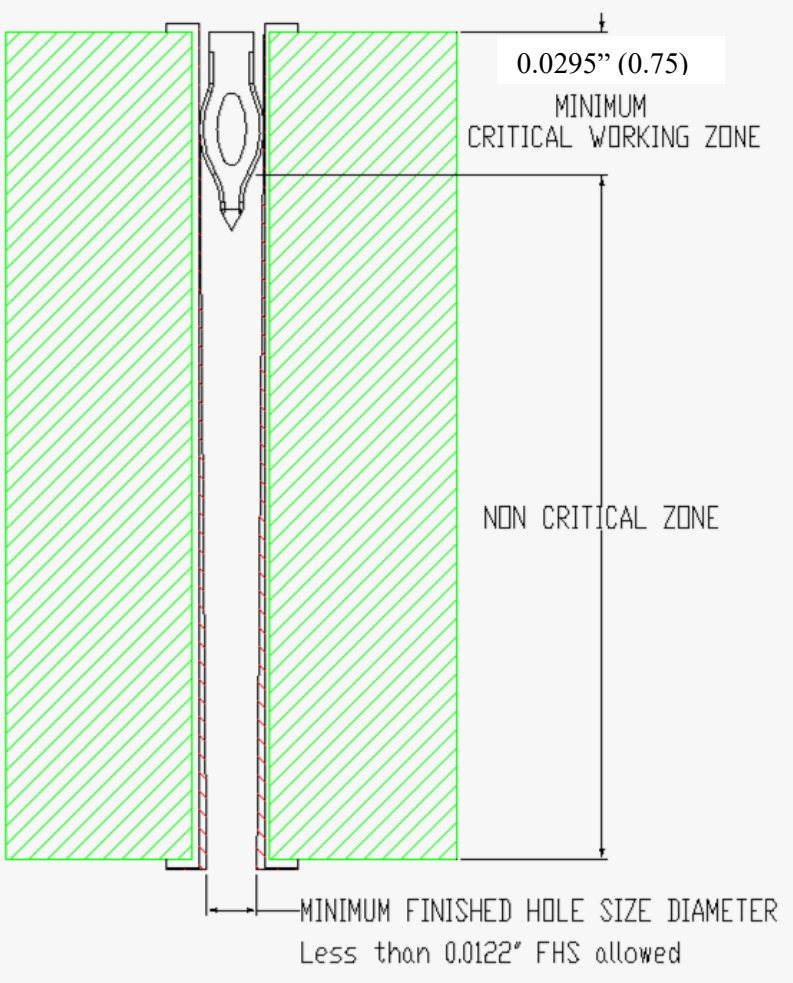

Figure 10: XCede® Femto (0.0157”) tail X2 Compliant Pin Critical Zone

5.8 Dual Diameter Via

The short tail compliant pin is particularly suited for use with dual-diameter vias, which should be considered for high speed signals. The larger diameter is drilled first to a controlled depth followed by the second smaller drill.

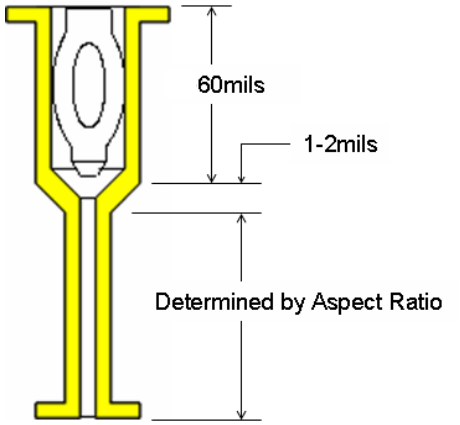

Figure 11: Diagram of a dual diameter via with the XCede® medium tail (0.0217”) compliant pin.

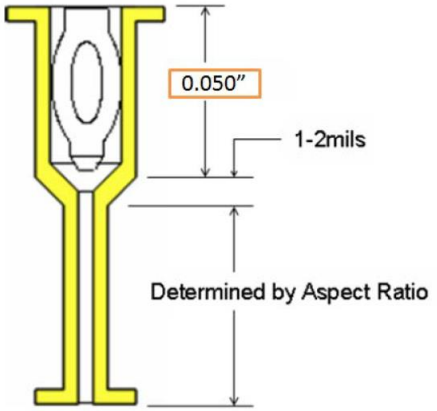

Figure 12: Diagram of dual diameter via with the X2 Femto tail (0.0157") compliant pin

5.9 Typical Anti-pad Geometry

The following describes the nominal antipad design for XCede® and XCede® Plus. Variations to this design based on stackup design and performance requirements are allowed.

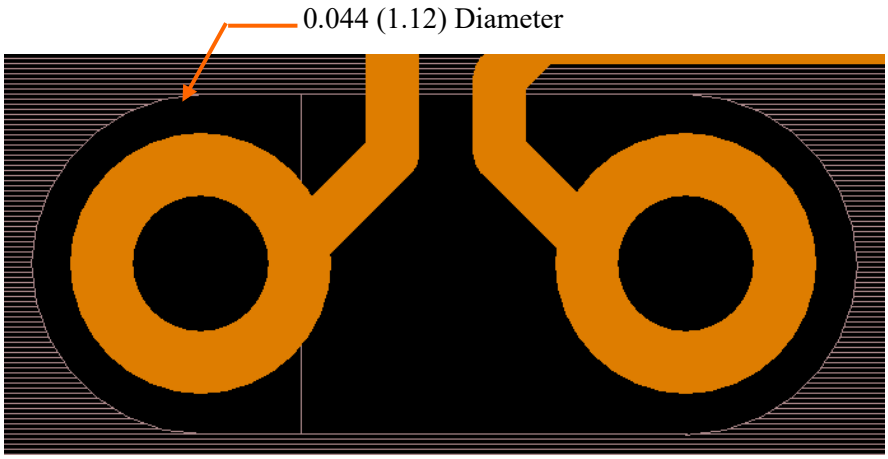

Figure 13: Antipad Clearance – XCede® and XCede® Plus Backplane Connector

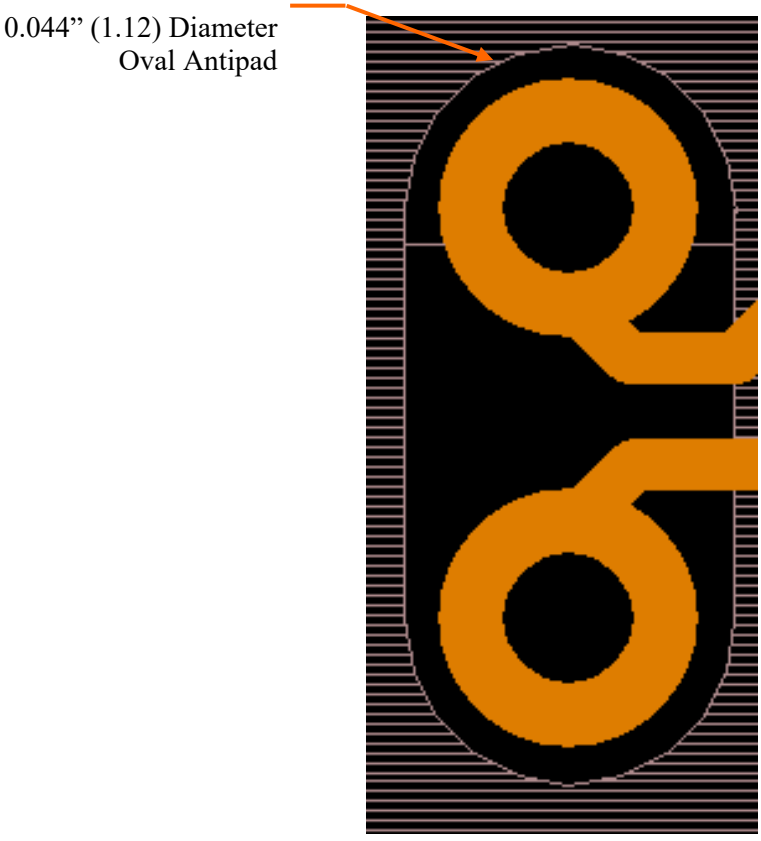

Figure 14: Antipad Clearance – XCede® and XCede® Plus Daughtercard Connector

See also section 5.9.3 and consult Amphenol TCS regarding usage of elongated Antipads for enhanced impedance

5.10 XCede®,XCede® Plus and XCede® X2 Typical High Speed Differential Routing

For complete hole pattern dimensions please refer to the customer use drawings.

5.10.1 Example XCede® and XCede® Plus Daughtercard Routing

The available space for routing is determined by the distance between antipads. *There is no secondary routing channel available on the Daughtercard for differential pairs.*

Center to Center	0.0728 (1.85)
- AntiPad Diameter	0.044 (1.12)
= Resulting Space for Traces	**0.0288 (0.732)**
Line Width	**0.007 (0.18)**
Space Between Lines	**0.007 (0.18)**
Resulting Ground Plane Web Overhang on Each Side	**0.004 (0.10)**

Table 7: Example XCede® and XCede® Plus Daughtercard Routing Channel

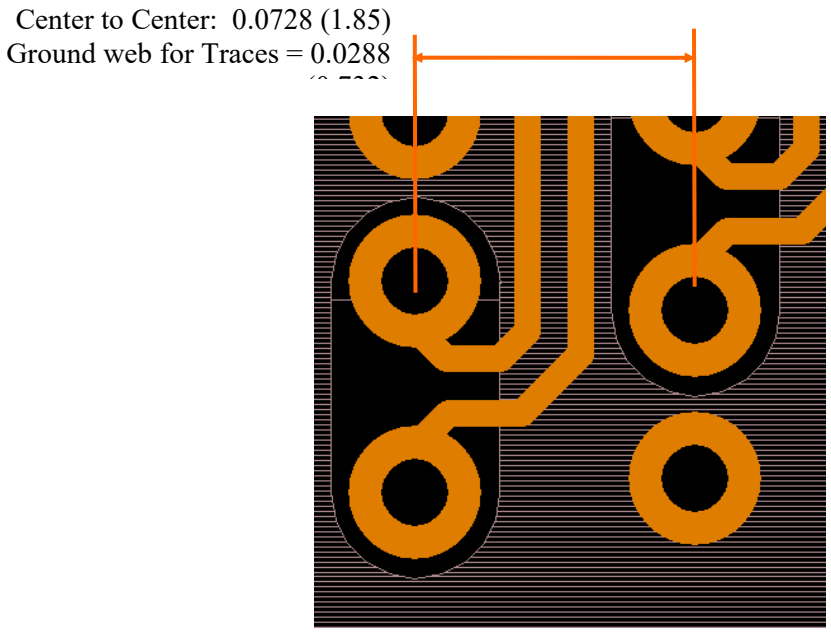

Figure 15: Example XCede® and XCede® Plus Daughtercard High Speed Differential Routing

5.10.2 Example X2 Daughtercard Routing

The available space for routing is determined by the distance between antipads. *There is no secondary routing channel available on the Daughtercard for differential pairs.*

Center to Center	0.0728 (1.85)
- AntiPad Diameter	0.046 (1.12)
= Resulting Space for Traces	**0.0268 (0.68)**
Line Width	**0.006 (0.152)**
Space Between Lines	**0.006 (0.152)**
Resulting Ground Plane Web Overhang on Each Side	**0.0044 (0.111)**

Table 8: Example X2 Daughtercard Routing Channel

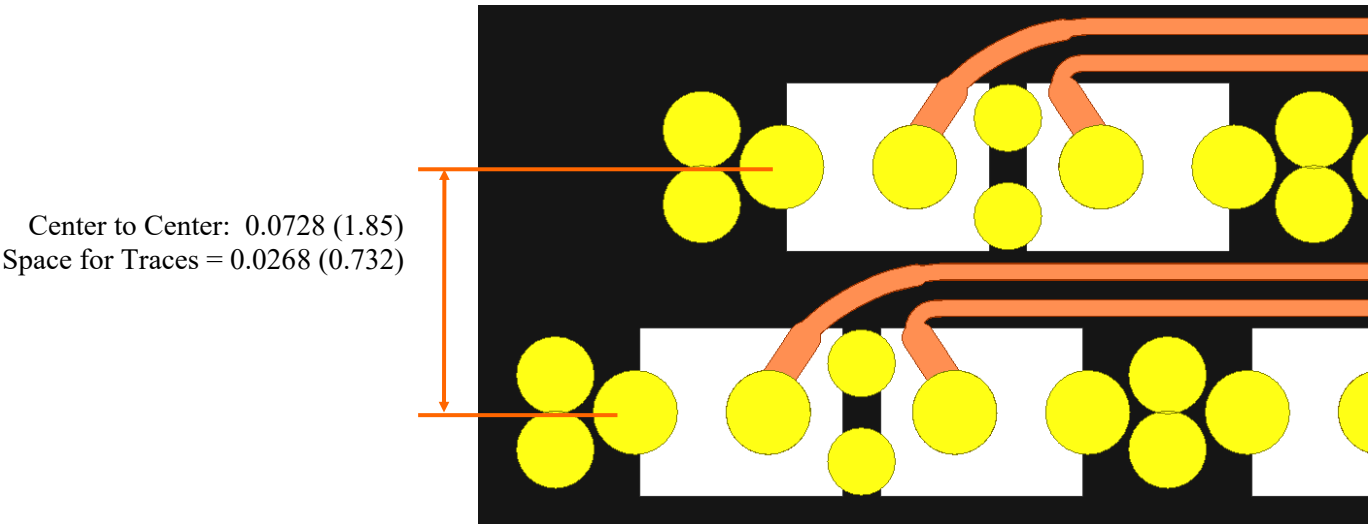

Figure 16: Example XCede X2® Daughtercard High Speed Differential Routing

5.10.3 X2 Daughtercard routing – Advanced features for improved signal integrity performance.

The X2 footprint assumes the use of individual rectangular antipads as shown in figure 14. The individual antipads, along with the pair of "shadow via's" greatly improve the footprints common mode performance.

Additionally, the use of the antipad shape shown on figure 14, placed directly below the routed diff pair, and making the un-coupled portion of the diff pair the corresponding width for the particular single ended impedance greatly helps with overall impedance matching and common mode performance.

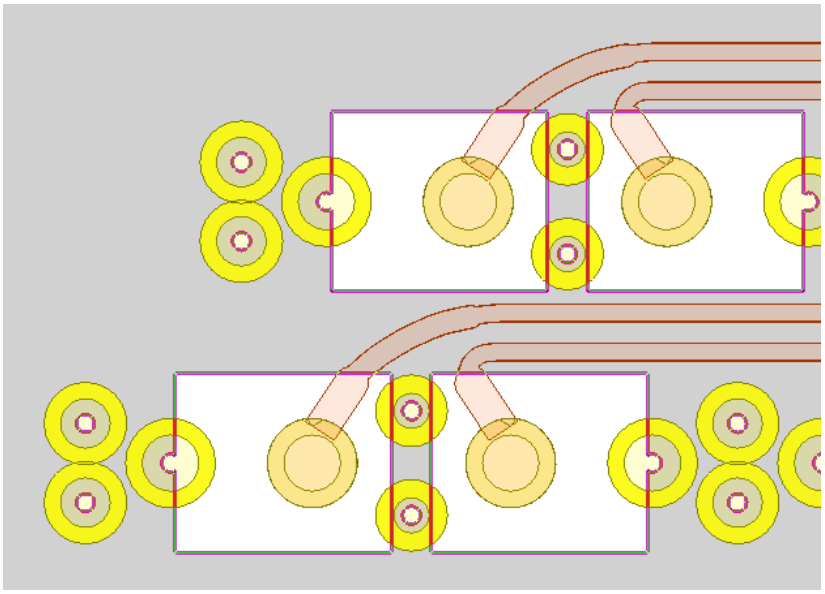

Figure 17: Example X2® Daughtercard Typical High Speed Differential antipad design

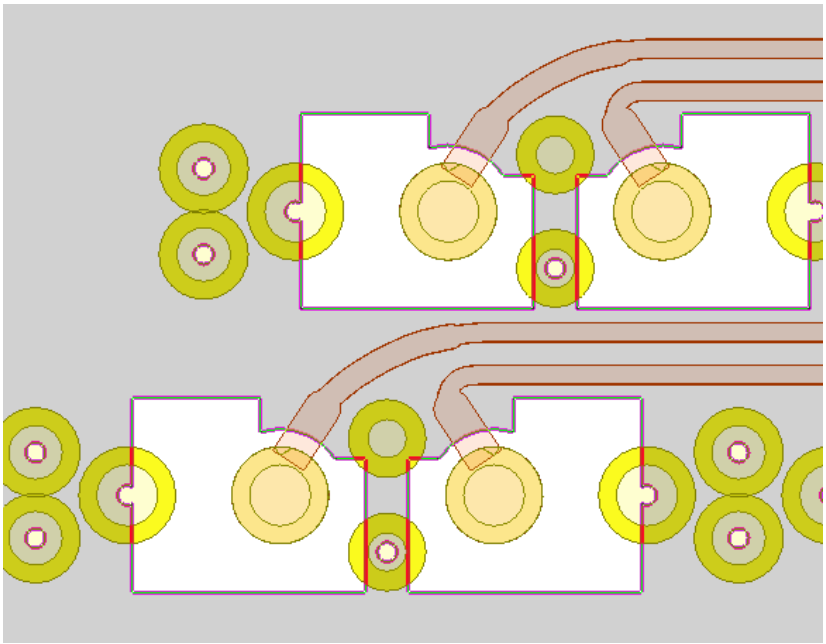

Figure 18: Example XCede X2® Daughter Card Typical High Speed Differential antipad design

5.10.4 Example XCede® and XCede® Plus Backplane Routing

The amount of space available for routing is determined by the ground plane web in between the antipad clearances.

Center to Center	0.0728 (1.85)
- AntiPad Diameter	0.044 (1.12)
= Resulting Space for Traces	**0.0288 (0.732)**
Line Width	**0.007 (0.18)**
Space Between Lines	**0.007 (0.18)**
Resulting Ground Plane Web Overhang on Each Side	**0.004 (0.10)**

Table 9: Example XCede® and XCede® Plus Backplane Primary (Horizontal) Routing Channel

Ground Pin Center to Center	0.06142 (1.560)
- Drill Diameter	0.0217 (0.551)
- Required Clearance to Barrel * 2	0.018 (0.46)
= Resulting Space for Traces	**0.0217 (0.551)**
Line Width	**0.007 (0.18)**
Space Between Lines	**0.007 (0.18)**

Table 10: Example XCede® Backplane Secondary (Vertical) Routing Channel

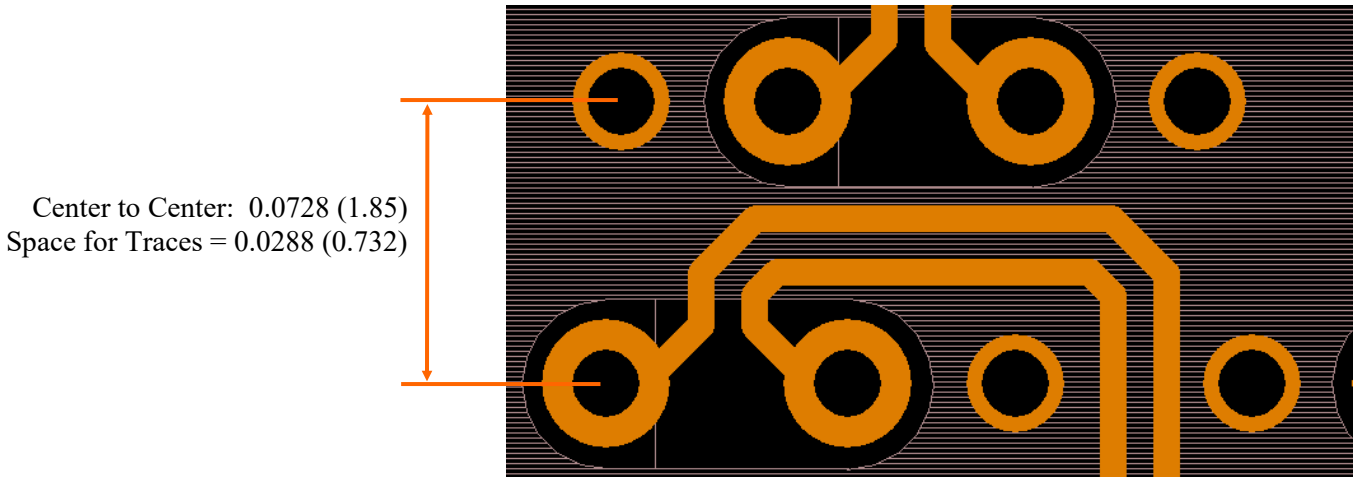

Figure 19: Example XCede® Backplane Typical High Speed Differential Routing. Ground Plane

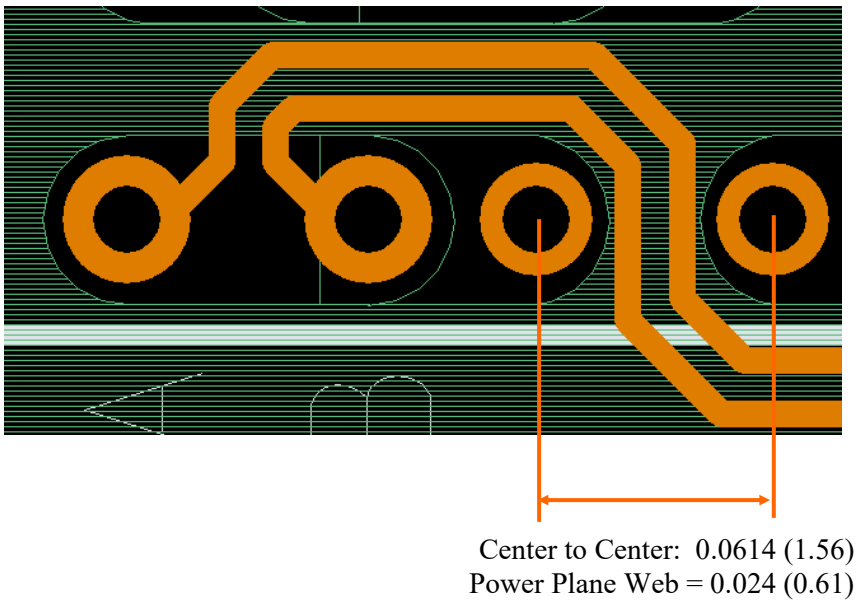

Figure 20: Example XCede® and XCede® Plus Backplane Typical High Speed Differential Routing Power Plane

5.10.1 Elongated Antipad for Improved Return Loss

The double ground vias between signal pairs in XCede® and XCede® Plus allow for elongated antipads that directly pass through the ground vias. There are two ways to achieve this antipad design. The first option, shown in Figure , has the antipad cut through the center of the ground vias. In this case a pad is needed at the ground via in order to ensure proper drill location.

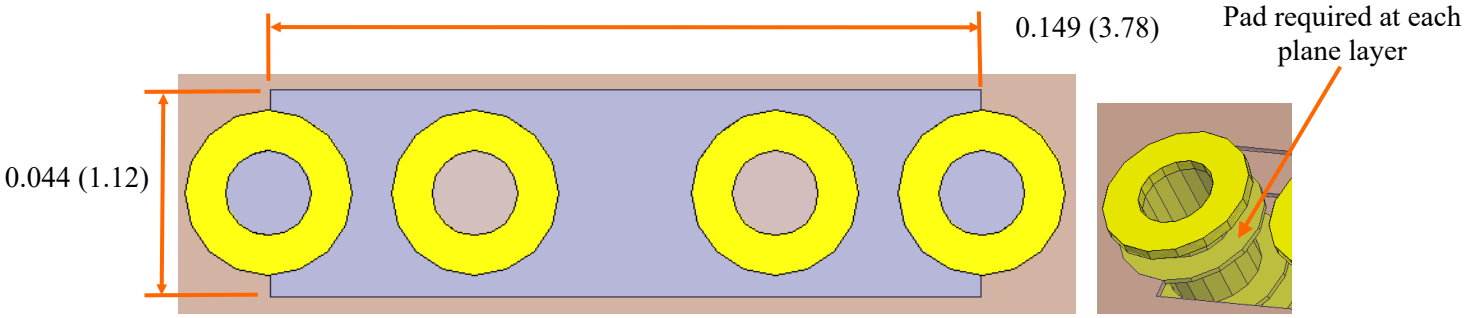

Figure 21: Option 1 Elongated Rectangular Backplane Antipad Clearance.

The second option, shown in Figure , uses an antipad that is 6mils shorter than the above case. A pad is not needed at the ground via because the drill bit will not wander from the ground via center when it strikes the plane.

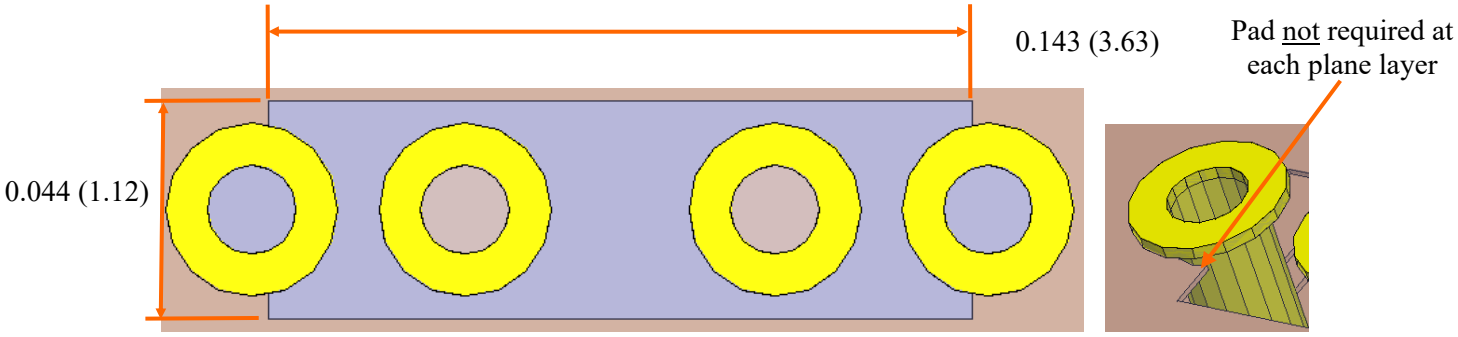

Figure 22: Option 2 Elongated Rectangular Backplane Antipad Clearance.

Figure shows the performance improvement in S11 by using the elongated rectangular antipad. This plot is from an HFSS simulation of a 24 layer backplane using Nelco 4000-13 with a 32mil stub.

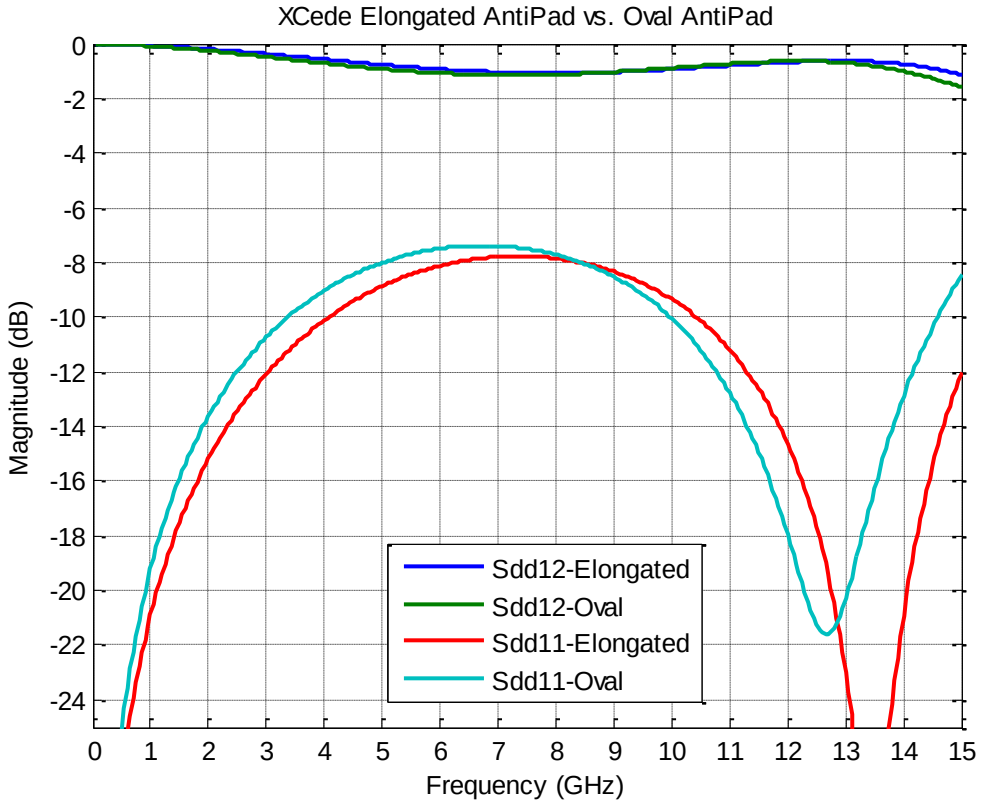

Figure 23: Performance Improvement of Elongated Antipad.

5.10.2 2-Layer Escape Routing with the XCede® 4-pair Connector

The following picture shows how to escape out of the 4-pair connector in only 2 layers. If this strategy is used, space for 7 pairs between connector modules is needed. 3 open teeth in the stiffener between connector modules are needed to fit 7 pairs using 5-6-5-20 spacing. 4 open teeth in the stiffener between connector modules are needed to fit 7 pairs using 7-7-7-27 spacing.

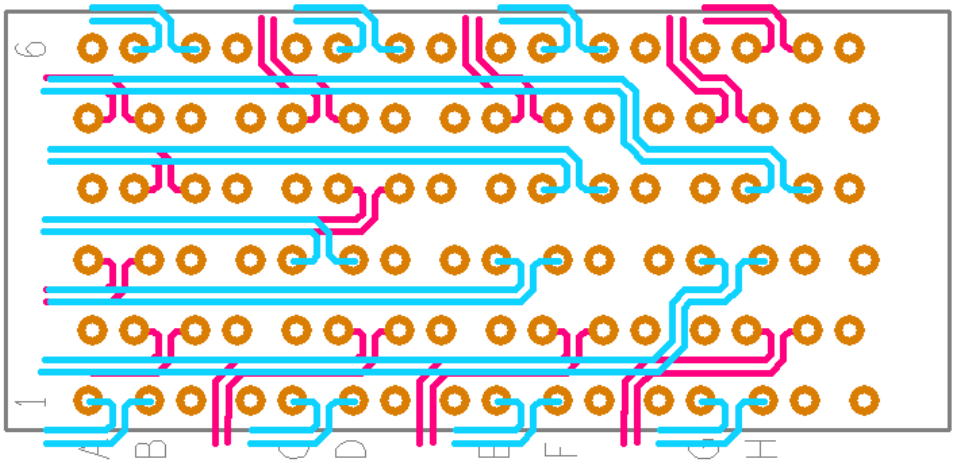

Figure 24: Example XCede® 4-pair 2-layer escape routing

5.10.3 Example X2 Backplane Routing

The amount of space available for routing is determined by the ground plane web in between the antipad clearances.

Center to Center	**0.0728 (1.85)**
- AntiPad Diameter	**0.046 (1.17)**
= Resulting Space for Traces	**0.0268 (0.68)**
Line Width	**0.007 (0.18)**
Space Between Lines	**0.007 (0.18)**
Resulting Ground Plane Web Overhang on Each Side	**0.003 (0.074)**

Table 11: Example X2 Backplane Primary (Horizontal) Routing Channel

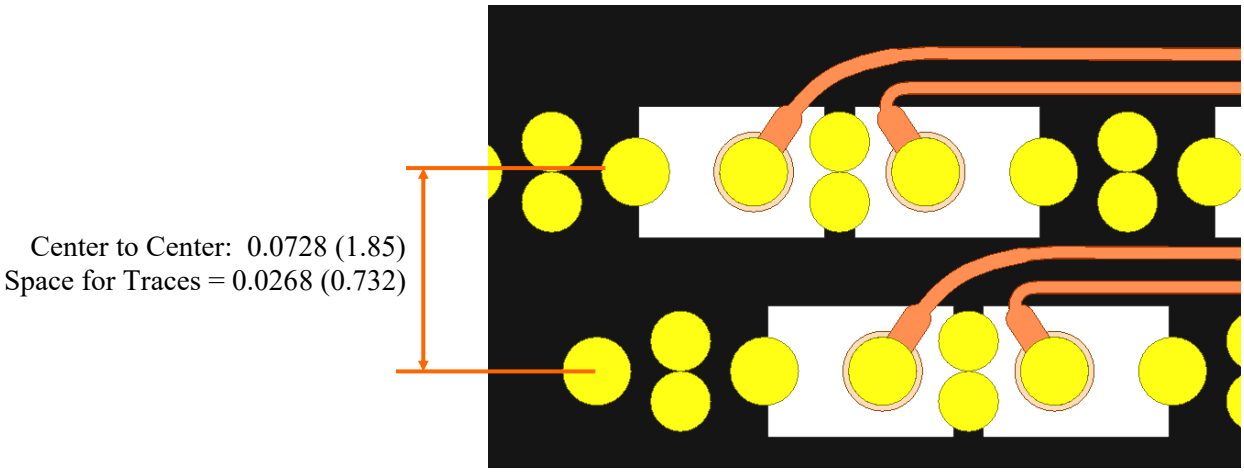

Figure 25: Example X2® Backplane Typical High Speed Differential Routing Ground Plane

5.10.4 **X2 Antipads**

The X2 footprint assumes the use of individual rectangular antipads as shown in figure 23. The individual antipads, along with the pair of “shadow vias” greatly improve the footprints common mode performance.

Additionally, the use of the antipad shape shown on figure 23, placed directly below the routed diff pair, and making the un-coupled portion of the diff pair the corresponding width for the particular single ended impedance greatly helps with overall impedance matching and common mode performance.

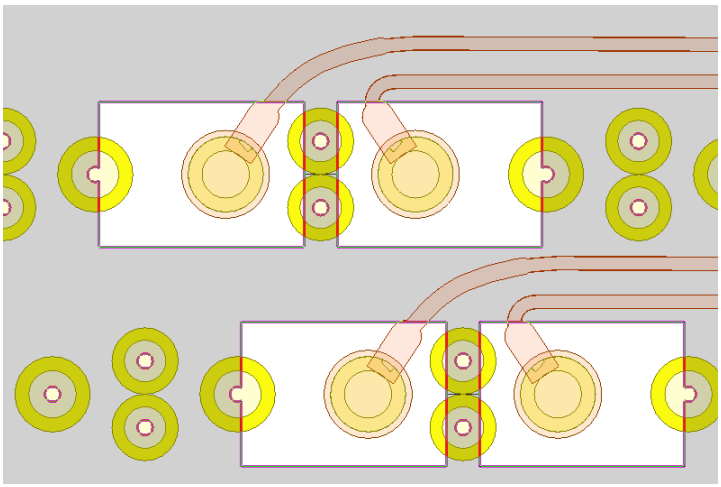

Figure 26: Example X2® Backplane Typical High Speed Differential antipad design

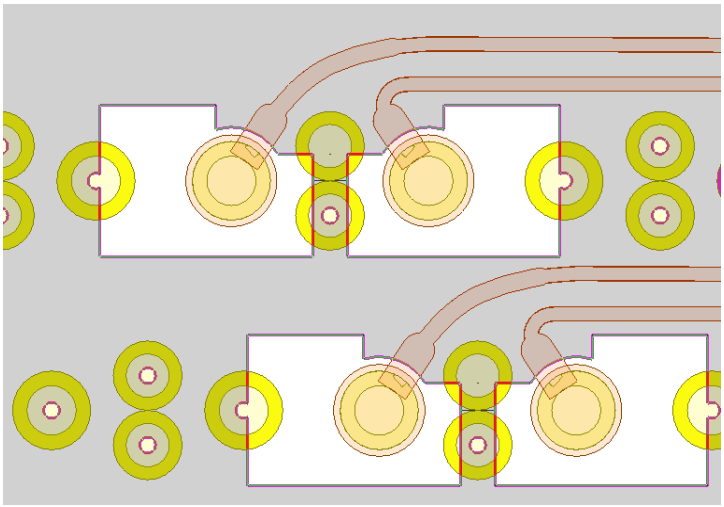

Figure 27: Example X2® Backplane Typical High Speed Differential antipad design

5.10.5 Printed Circuit Board Skew Compensation

If the length of one net of a differential pair needs to be increased in order to achieve low skew within the pair, the following picture shows an example of how to achieve this goal.

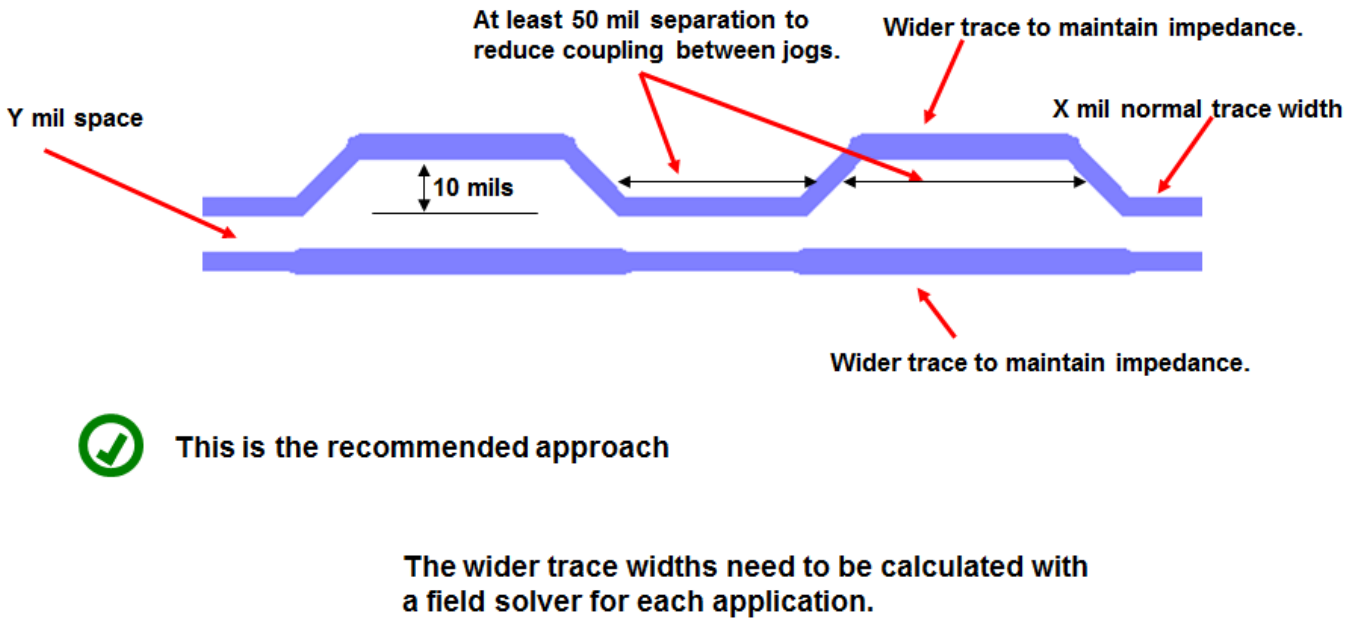

Figure 28: Skew compensation recommended approach

6. Midplane Applications

The XCede connector can be used in a midplane application where vias are “shared” between front and rear cards. The front and rear cards must be “coplanar” meaning the front and rear card guides must line up. The connectors must be offset by 1 column and front card pin numbering sequence is opposite from rear card pin numbering sequence.

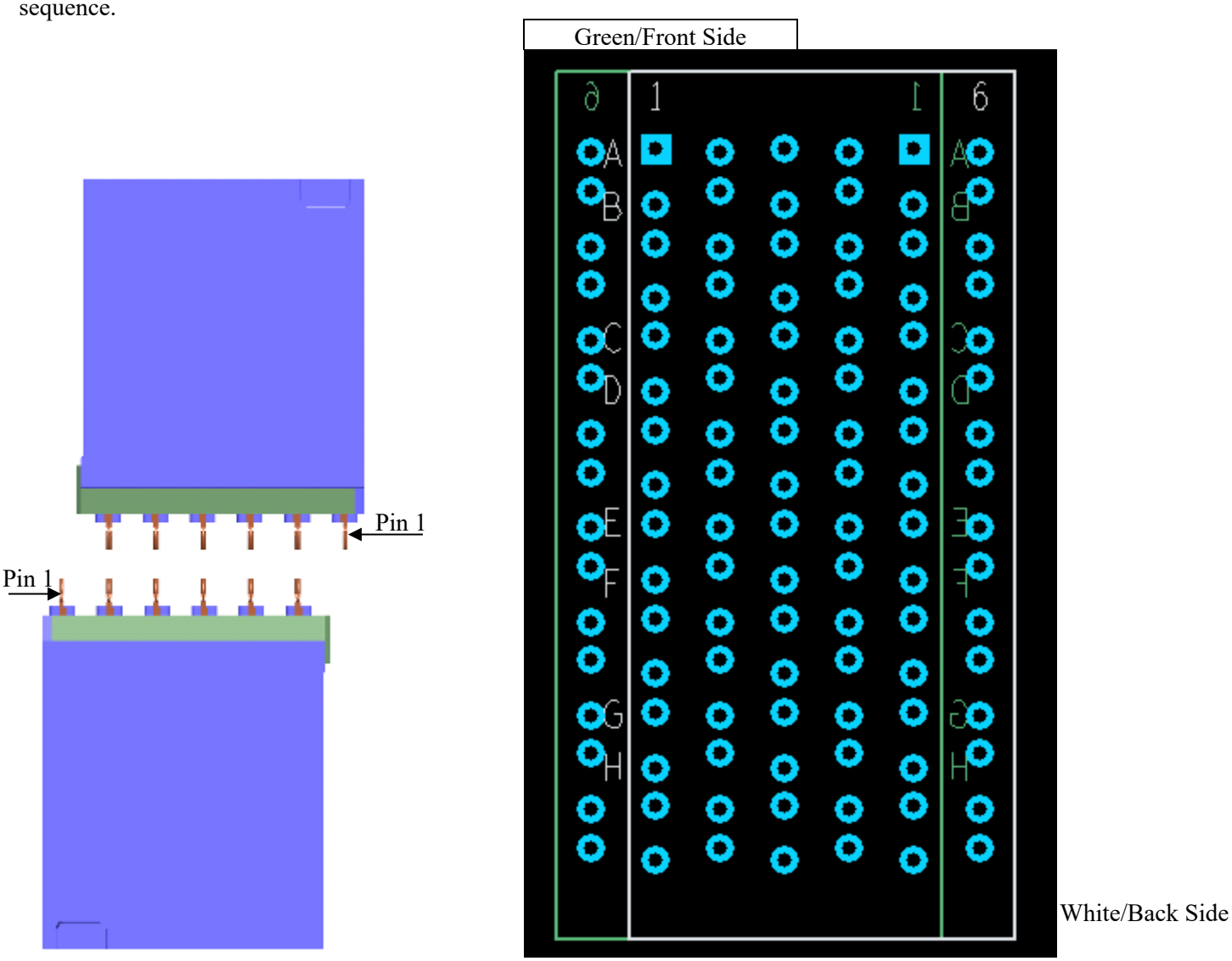

Figure 29: Example XCede® Midplane Connector