TB-2237

XCede® HD Family Routing Guidelines

Revision “N”

1. Specification Revision Status

Revision	SCR No.	Description	Initial	Date
“L”	S4932	Updated section 5.2.5,specified keep out zone	B.Wang	09-09-2016
“M”	S5810	Updated figure8 Minimum critical working zone value. Updated figure 10,11,12,13 antipad dimension.	B.Wang	05/22/2017
“N”	S7821	Added XHD2 routing guideline.	B.Wang	07/25/2019

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2. Scope

2.1 Intent

The intent of this technical bulletin is to outline the standard signal trace widths, minimum spacing requirements, and finish hole size requirements for the XCede® HD connector series when used in differential signal applications and low speed applications. This document supercedes all other XCede® HD documents including customer use drawings when conflicts exist for the stated requirements outlined within this document.

2.2 Efficient routing

Efficient routing of signal traces between connector patterns improves yields and manufacturability. Spacing between trace/pad and trace/trace needs to be considered to allow for proper feature modifications needed for the inner layer fabrication process. Failure to allow for this may result in lower yields and higher PWB costs.

2.3 Finished Hole Sizes

All finished hole size requirements provided within this document are based on testing completed in FR-4 laminate.

3. Definitions

3.1 Fillets

An extension of the pad at the interface of the trace to the pad that will allow more pad area, in the event that the pad to hole registration compromises the interconnect area. See Figure 1 for details. For further information regarding these routing guidelines, please contact ATCS Applications Engineering.

3.2 Foils/Copper Weights

Copper foil is measured in ounces (or weight). Common copper weights are 0.5 ounces, 1 ounce, 1.5 ounces and 2 ounces (3 ounces up to 10 ounces are available for special order). 1 ounce = 0.0014”, 1.5 ounces = 0.0021”, 2 ounces = 0.0028”.

3.3 Pads/Lands/Annular Ring

A pad is the target geometry for incoming traces. If you see a specification calling out an annular ring of 0.005”, that will mean the amount of the pad left around the hole after processing.

3.4 Spacing

Spacing is the space between two electrical connections; it can be between two lines, two pads, a line and a pad etc.

3.5 Trace/Circuit/Line Width/Lines/Conductor

These are different terms for a connection. If you see the term 0.008” lines, it means the electrical connection from one point to another will measure 0.008” width.

3.6 Vertical Header or Right Angle Male (RAM)

When used within this document refers to the PCB associated with the male connector half of the connector system mounted to a fixed pcb in a chassis.

3.7 Right Angle Receptacle or Stacker (Mezzanine)
When used within this document refers to the PCB associated with the female connector half of the connector system mounted to a plug-in card in a chassis.

4. Routing Guidelines

4.1 Minimum Spacing
Minimum spacing, specific pad/trace, and trace/trace between all features should be 0.005” (0.127) to allow for manufacturing tolerances.

4.2 Impedance
Consider characteristic impedance (if applicable) when designing to ensure line widths will meet requirements. Please contact ATCS Application Engineering for impedance calculations.

4.3 Copper Weights
Consider copper weights when routing. Higher weights will impact minimum trace widths.

4.4 Fillets
Fillets at the interface (egress) of the trace to the pad are required to improve annular ring when the electrical design requires tight hole to pad configurations.

4.5 Trace Centering
Center all traces between holes to optimize spacing.

4.6 Non Functional Pads
For high speed applications, remove all non-functional pads.

5. Design Rules and Manufacturability Guidelines

5.1 General Design Rules

5.1.1 PCB Compliant Pin Drill Size
15.7mil Hole: ISO 0.40mm (0.0157”).
17.7mil Hole: ISO 0.45mm (0.0177”).
21.7mil Hole: ISO 0.55mm (0.0217”).

5.1.2 Footprint
For specific connector footprint see customer use drawings.

5.1.3 Drilled Hole and Copper Thickness
For copper wall thickness requirements and finished hole size reference, see Table 4, Figure 2, Figure 3 and Figure 4.

5.2 Daughtercard/Backplane Manufacturability Guidelines

5.2.1 Line Widths, Pad Sizes and Spacing
Line widths, pad sizes and spacing applicable for 1/2 ounce and 1 ounce copper weights.

5.2.2 Filleting

Filleting of pads recommended (to be added by fabricator) for 0.000” annular ring (tangency), see Figure 1.

5.2.3 Minimum PCB Thickness

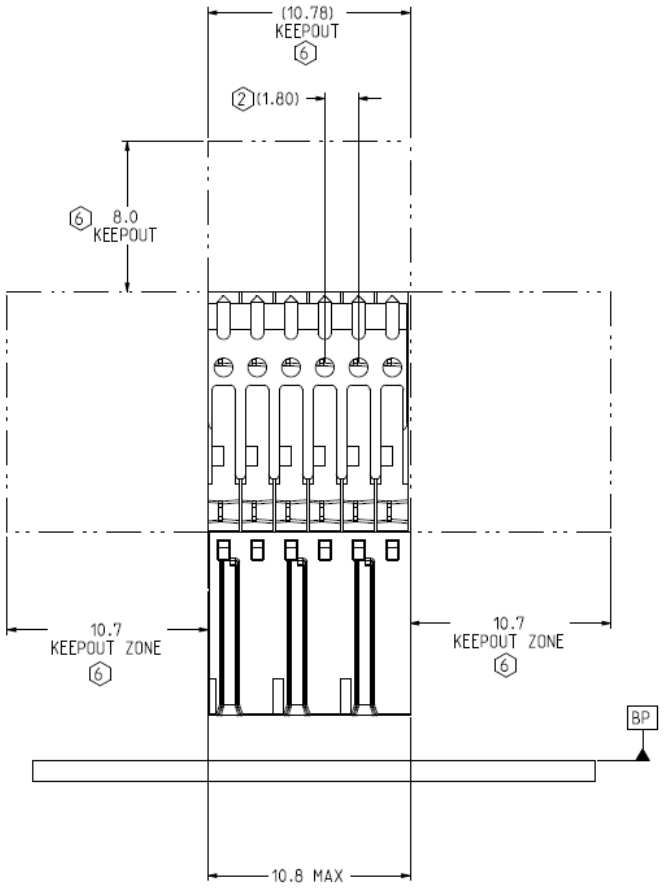
21.7mil: Recommended minimum PCB thickness of 0.043” (1.1mm).
17.7mil: Recommended minimum PCB thickness of 0.043” (1.1mm).
15.7mil: Recommended minimum PCB thickness of 0.043” (1.1mm).

5.2.4 Plane Clearances

Plane clearances are applicable for copper weights up to 2 ounces. Please contact ATCS Application Engineering for applications with more than 2 ounce copper.

5.2.5 Surface Traces and keep out zones

Surface traces are not recommended. If surface traces are used refer to the customer drawings for keep-out zones, for Daughtercard, please refer to C922-,C954-,C915- & C919- series drawings, for Backplane, please refer to C1900009000.



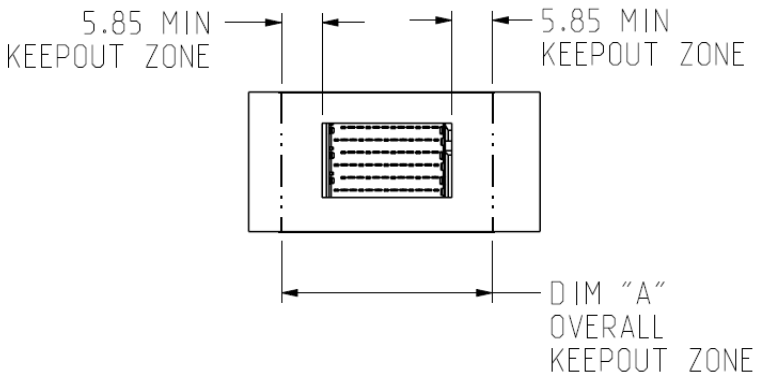


Figure 1: keep out zone for reference

6. Routing Guidelines

6.1 XCede® HD , XCede® HD Plus and XCede® HD2 15.7mil Drill Signal Pad Sizes

PCB Material Thickness, in (mm)	Copper Weight Ounces	Process	Min. Pad Size 0.000 A/R, in (mm)	Min. Pad Size 0.001 A/R, in (mm)	Min. Pad Size 0.002 A/R, in (mm)
0.035 to 0.400 (1.1 to 10.16)	0.5 (17µm)	Inner Layer	0.026 (0.66)	0.028 (0.71)	0.030 (0.76)
		Outer Layer	0.028 (0.71)	0.030 (0.76)	0.032 (0.81)
0.035 to 0.400 (1.1 to 10.16)	1.0 (35µm)	Inner Layer	0.027 (0.79)	0.029 (0.74)	0.031 (0.79)
		Outer Layer	0.029 (0.68)	0.031 (0.79)	0.033 (0.84)
0.035 to 0.400 (1.1 to 10.16)	2.0 (70µm)	Inner Layer	0.029 (0.68)	0.031 (0.79)	0.034 (0.86)
		Outer Layer	0.031 (0.79)	0.033 (0.84)	0.035 (0.89)

Table 1: XCede® HD , XCede® HD Plus and XCede® HD2 15.7mil Drill Minimum Pad Size vs. Copper Weight and Annular Ring (“A/R”)

Notes for Table 1:

1. Outer layer pad sizes reflect panel plating process.
2. Use inner layer pad sizes for outers when pattern plating.
3. Values in ( ) are metric equivalents. For printed circuit board layout use metric units.

6.2 XCede® HD and XCede® HD Plus 17.7mil Drill Signal Pad Sizes

PCB Material Thickness, in (mm)	Copper Weight Ounces	Process	Min. Pad Size 0.000 A/R, in (mm)	Min. Pad Size 0.001 A/R, in (mm)	Min. Pad Size 0.002 A/R, in (mm)
0.043 to 0.400	0.5 (17μm)	Inner Layer	0.03 (0.76)	0.032 (0.81)	0.034 (0.86)
(1.07 to 10.16)		Outer Layer	0.032 (0.81)	0.034 (0.86)	0.036 (0.91)
0.043 to 0.400	1.0 (35μm)	Inner Layer	0.031 (0.79)	0.033 (0.84)	0.035 (0.89)
(1.07 to 10.16)		Outer Layer	0.033 (0.84)	0.035 (0.89)	0.037 (0.94)
0.043 to 0.400	2.0 (70μm)	Inner Layer	0.033 (0.84)	0.035 (0.89)	0.037 (0.94)
(1.07 to 10.16)		Outer Layer	0.035 (0.86)	0.037 (0.91)	0.039 (0.99)

Table 2: XCede® HD and XCede® HD Plus 17.7mil Drill Minimum Pad Size vs. Copper Weight and Annular Ring ("A/R")

Notes for Table 2:

1. Outer layer pad sizes reflect panel plating process.
2. Use inner layer pad sizes for outers when pattern plating.
3. Values in ( ) are metric equivalents. For printed circuit board layout use metric units.

6.3 XCede® HD 21.7mil Signal Pad Sizes

PCB Material Thickness, in (mm)	Copper Weight Ounces	Process	Min. Pad Size 0.000 A/R, in (mm)	Min. Pad Size 0.001 A/R, in (mm)	Min. Pad Size 0.002 A/R, in (mm)
0.043 to 0.400	0.5 (17μm)	Inner Layer	0.034 (0.86)	0.036 (0.91)	0.038 (0.97)
(1.07 to 10.16)		Outer Layer	0.036 (0.91)	0.038 (0.97)	0.04 (1.02)
0.043 to 0.400	1.0 (35μm)	Inner Layer	0.035 (0.89)	0.037 (0.94)	0.039 (0.99)
(1.07 to 10.16)		Outer Layer	0.037 (0.94)	0.039 (0.99)	0.041 (1.04)
0.043 to 0.400	2.0 (70μm)	Inner Layer	0.037 (0.94)	0.039 (0.99)	0.041 (1.04)
(1.07 to 10.16)		Outer Layer	0.039 (0.99)	0.041 (1.04)	0.043 (1.09)

Table 3: XCede® HD 21.7mil Drill Minimum Pad Size vs. Copper Weight and Annular Ring ("A/R")

Notes for Table 3:

1. Outer layer pad sizes reflect panel plating process.
2. Use inner layer pad sizes for outers when pattern plating.
3. Values in ( ) are metric equivalents. For printed circuit board layout use metric units.

6.4 Copper Thickness Requirement and Plated Through Hole Finish Thickness Reference

Finish Type	Copper thickness, in (mm) per side	Drill size, in (mm)	Typical Finish Thickness	Finished Hole Size, in (mm)
Lead Free HASL(1)	0.0010 (0.0254) min 0.0025 (0.0635) max	22.5mil: 0.0225 (0.57)	500 micro inches maximum	0.019 +0.0015/-0.002 (0.48+0.0381/-0.05)
Solder Finish (2)	0.0010 (0.0254) min 0.0025 (0.0635) max 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	21.7mil: 0.0217 (0.55) 17.7mil: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	300 to 500 micro inches	0.0177 +/- 0.002 (0.45 +/- 0.05) 0.0142 +/- 0.002 (0.36 +/- 0.05) Femto Tail: 0.0122+/- 0.002 (0.31+/-0.05)
Immersion Sn (Tin)	0.0010 (0.0254) min 0.0025 (0.0635) max 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	21.7mil: 0.0217 (0.55) 17.7mil: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	35 to 75 micro inches minimum	0.0177 +/- 0.002 (0.45 +/- 0.05) 0.0142 +/- 0.002 (0.36 +/- 0.05) Femto Tail: 0.0122+/- 0.002 (0.31+/-0.05)
Immersion Ag (Silver)	0.0010 (0.0254) min 0.0025 (0.0635) max 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	21.7mil: 0.0217 (0.55) 17.7mil: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	4 micro inches minimum	0.0177 +/- 0.002 (0.45 +/- 0.05) BP: 0.0142 +/- 0.002 (0.36 +/- 0.05) DC: 0.0142 +0.002/- 0.002 (0.36 +.05/- 0.05) Femto Tail: 0.0122+/- 0.002 (0.31+/-0.05)
Copper - OSP	0.0010 (0.0254) min 0.0025 (0.0635) max (DC) 0.0030 (0.0762) max (BP) 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	21.7mil: 0.0217 (0.55) 17.7mil: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	N/A	0.0177 +/- 0.002 (0.45 +/- 0.05) 0.0142 +/- 0.002 (0.36 +/- 0.05) Femto Tail: 0.0122+/- 0.002 (0.31+/-0.05)
Ni Au (Nickel-Gold)	0.0010 (0.0254) min 0.0025 (0.0635) max 0.0008 (0.020) min Femto tail 0.00275 (0.069) max Femto tail	21.7mil: 0.0217 (0.55) 17.7mil: 0.0177 (0.45) Femto Tail: 0.0157 (0.40)	53 to 210 micro inches Ni-Au compositions combined	0.0177 +/- 0.002 (0.45 +/- 0.05) BP: 0.0142 +/- 0.002 (0.36 +/- 0.05) DC: 0.0142 +0.002/- 0.002 (0.36 +.05/- 0.05) Femto Tail: 0.0122+/- 0.002 (0.31+/-0.05)

Table 4: Copper Thickness Requirement and Plated Through Hole Finish Thickness Reference

Notes:

1. Lead Free HASL uses larger drill size than other finishes (ex 21.7mil drill for Cu-OSP is 22.5mil for Pb-free HASL)
2. Solder finish includes: Tin/lead reflowed (plated and reflowed) and HASL

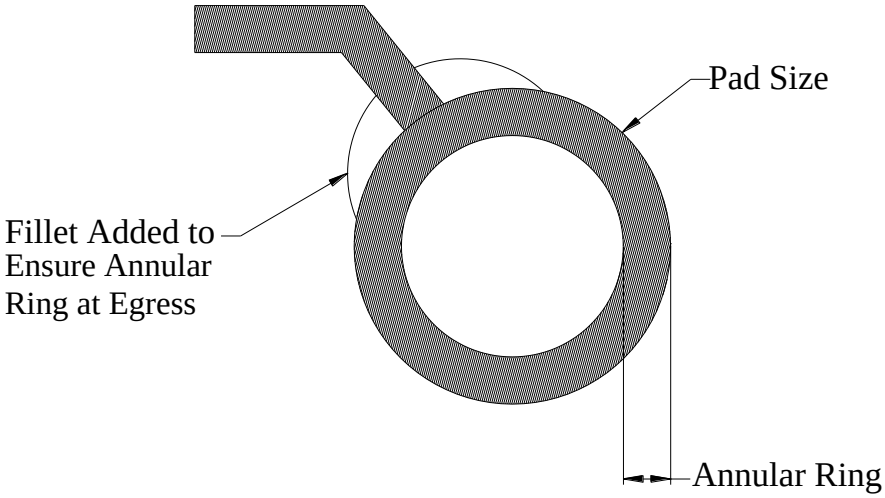


Figure 2: Preferred Fillet

Fillet diameter equals one half size of plated through hole pad diameter located on a line central to trace so that fillet size equals minimum annular ring plus 0.005” (0.13).

6.5 Drill and Finished Hole Size

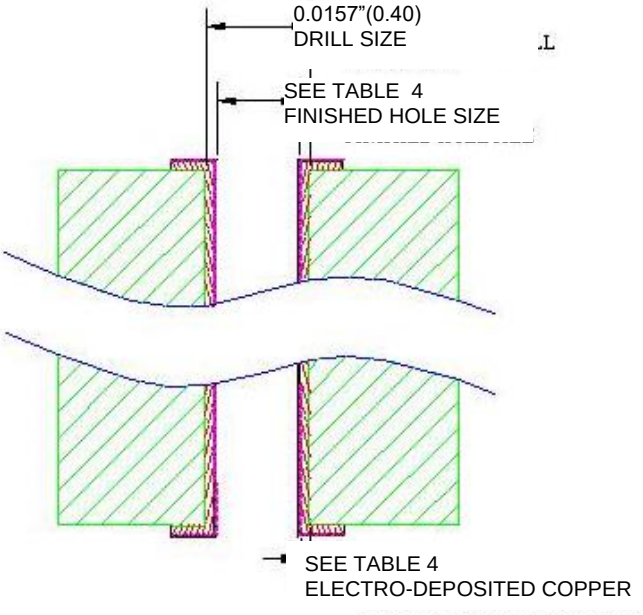


Figure 3: XCede® HD, XCede® HD Plus and XCede® HD2 15.7mil Drill and Finished Hole Size

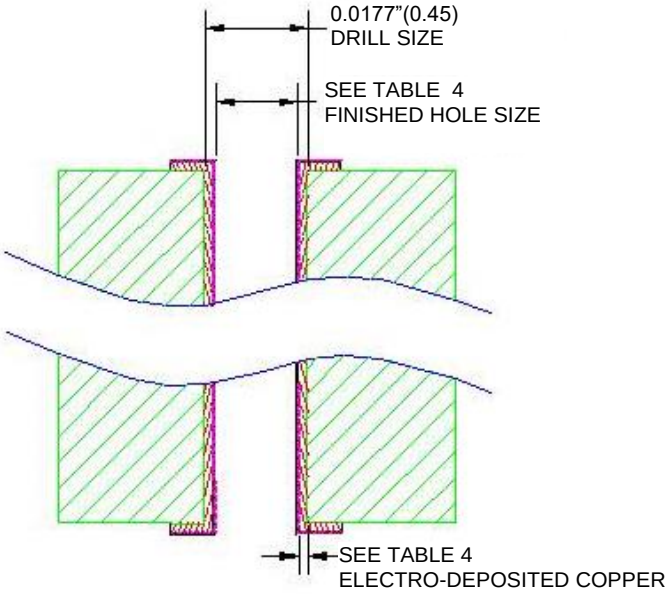


Figure 4: XCede® HD and XCede® HD Plus 17.7mil Drill and Finished Hole Size

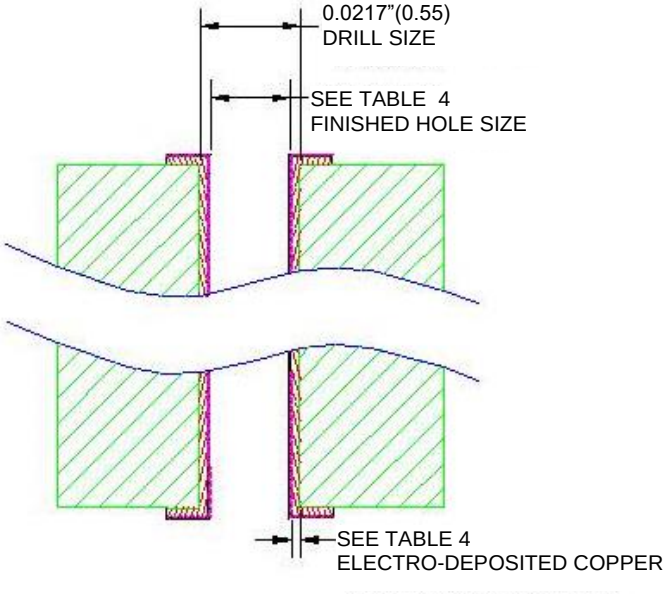


Figure 5: XCede® HD 21.7mil Drill and Finished Hole Size

6.6 Compliant Pin Critical Zone

The “Critical Working Zone” shown in the following figures is defined as the compliant working zone where the plated through hole requirements must meet the specifications defined within this document. In the “Non Critical Zone”, the plated through hole is allowed to go below the minimum required finish hole size for non midplane applications. Back drilling is allowed in the “non critical zone” only.

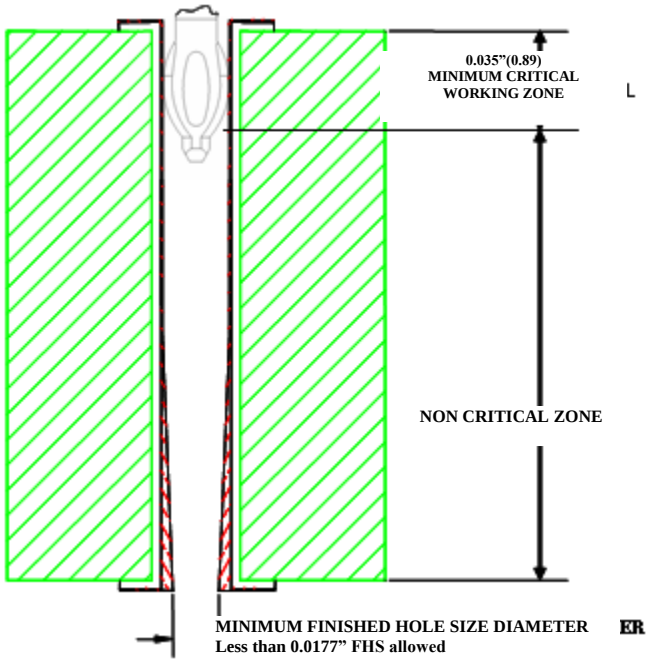


Figure 6: XCede® HD 21.7mil Compliant Pin Critical Zone

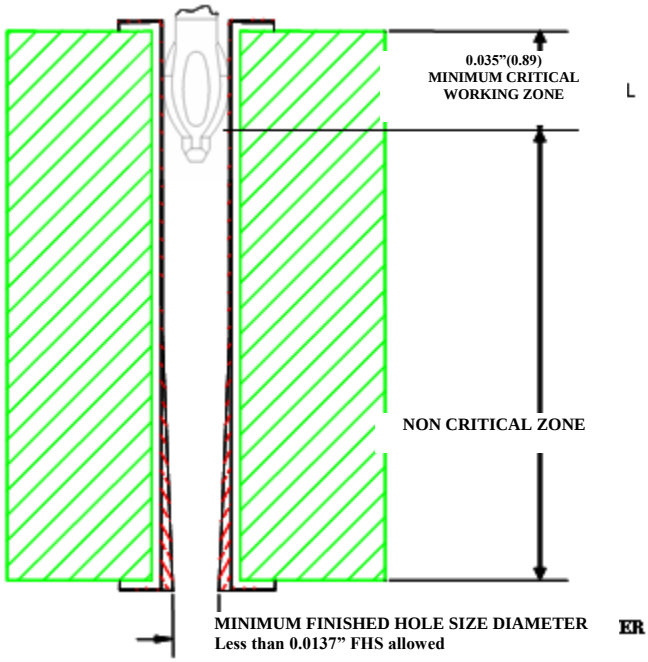


Figure 7: XCede® HD and XCede® HD Plus 17.7mil Compliant Pin Critical Zone

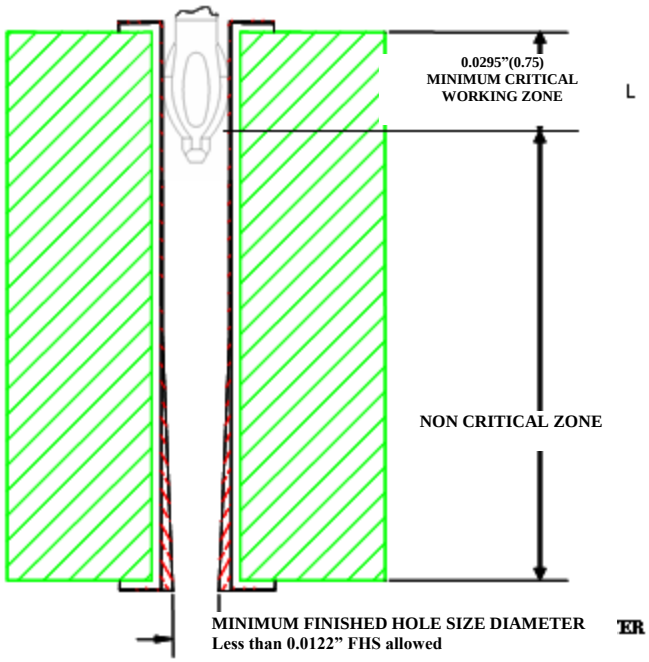


Figure 8: XCede® HD, XCede® HD Plus and XCede® HD2 15.7mil Compliant Pin Critical Zone

6.7 Dual Diameter Via

Both compliant pins are particularly suited for use with dual-diameter vias, which should be considered for high speed signals. The larger diameter is drilled first to a controlled depth followed by the second smaller drill. The smaller drill diameter is determined by allowable aspect ratio of the PCB.

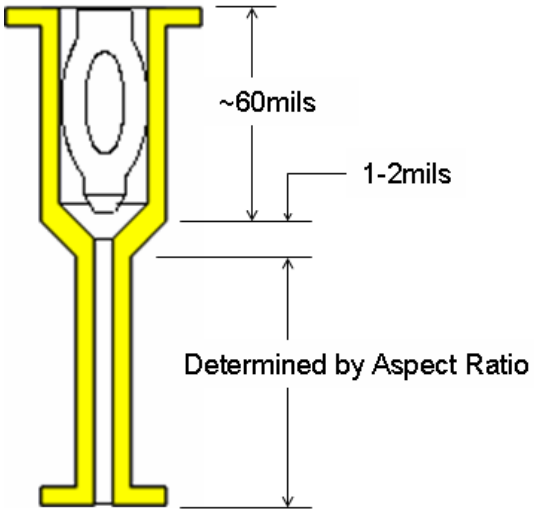


Figure 9: Diagram of a dual diameter via with the XCede® HD compliant pin

6.8 Typical Anti-pad Geometry

The following describes the nominal antipad design for XCede® HD. Variations to this design based on stackup design and performance requirements are allowed.

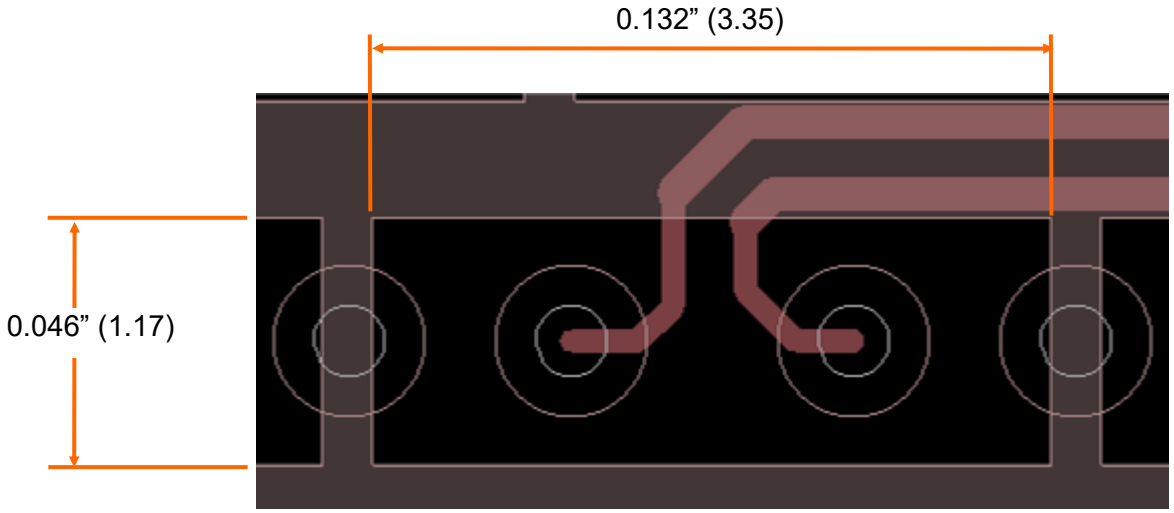


Figure 10: Antipad Clearance – XCede® HD & XCede® HD Plus Backplane Connector

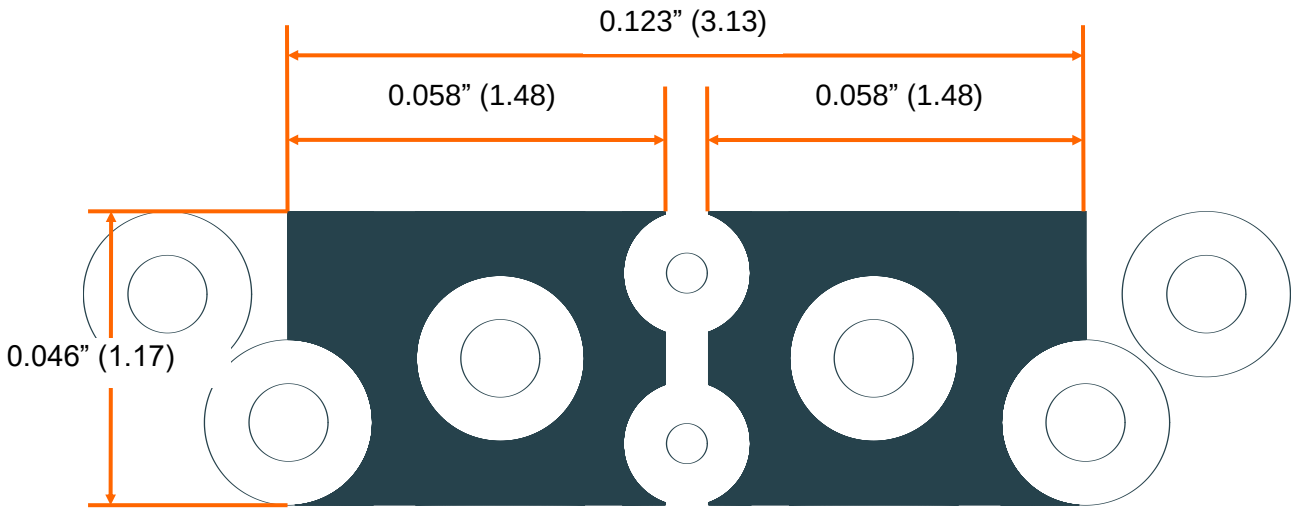


Figure 11: Antipad Clearance – XCede® HD2 Backplane Connector

The XCede HD2 footprint assumes the use of individual rectangular antipads as shown in figure 11. The individual antipads, along with the pair of “shadow via’s” greatly improve the footprints crosstalk and common mode performance.

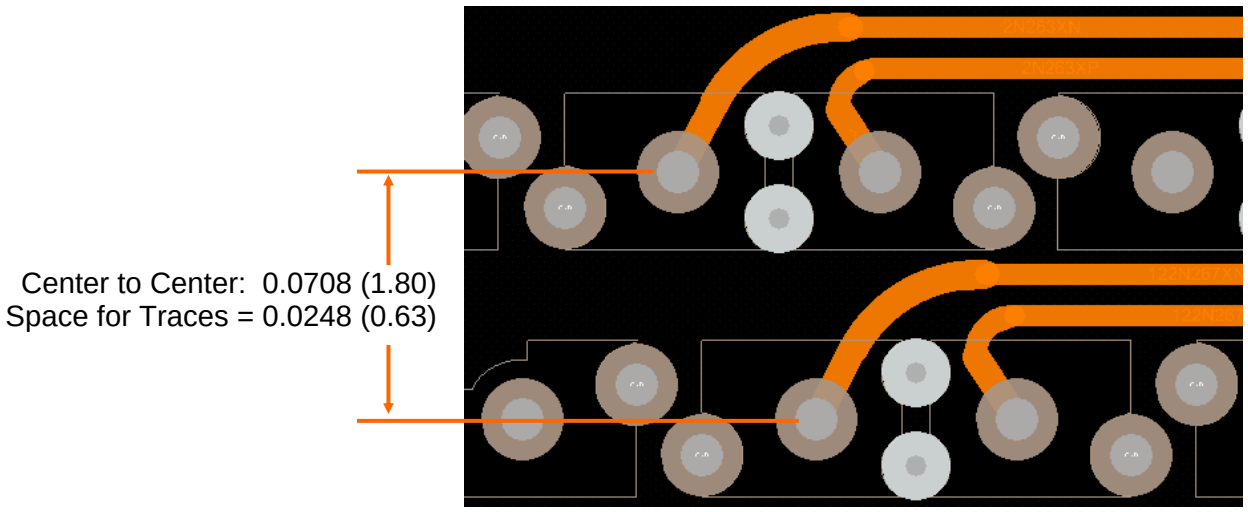


Figure 12: XCede® HD2 Backplane Typical High Speed Differential antipad design

Additionally, the use of the antipad shape shown on figure 12, placed directly below the routed diff pair, and making the un-coupled portion of the diff pair the corresponding width for the particular single ended impedance also greatly help with overall impedance matching and as mentioned common mode performance.

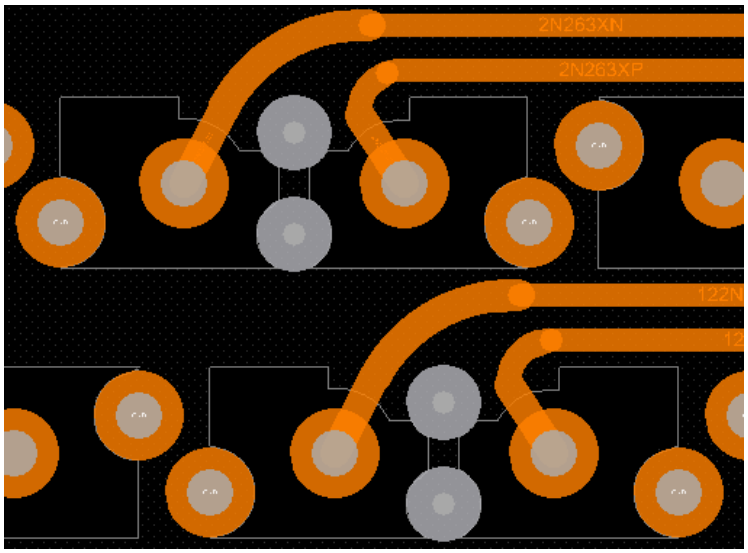


Figure 13: XCede® HD2 Backplane Typical High Speed Differential antipad design advance

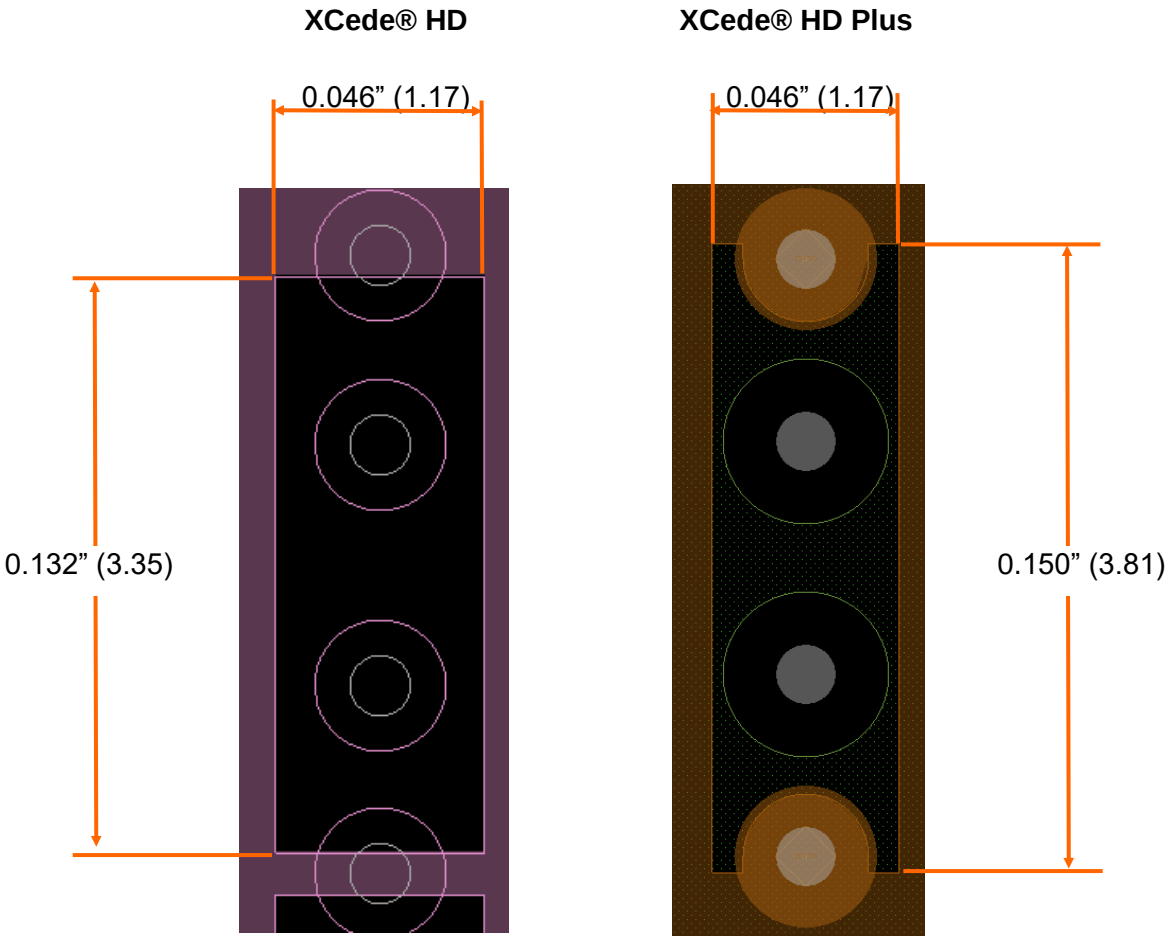


Figure 14: Antipad Clearance – XCede® HD and XCede® HD Plus Daughtercard Connector

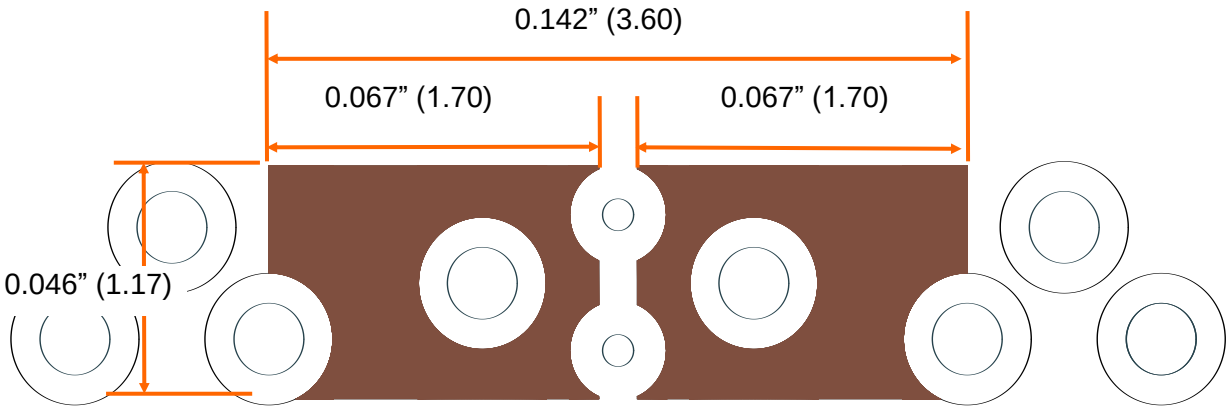


Figure 15: Antipad Clearance – XCede® HD2 Daughtercard Connector

The XCede HD2 footprint assumes the use of individual rectangular antipads as shown in figure 15. The individual antipads, along with the pair of “shadow via’s” greatly improve the footprints crosstalk and common mode performance.

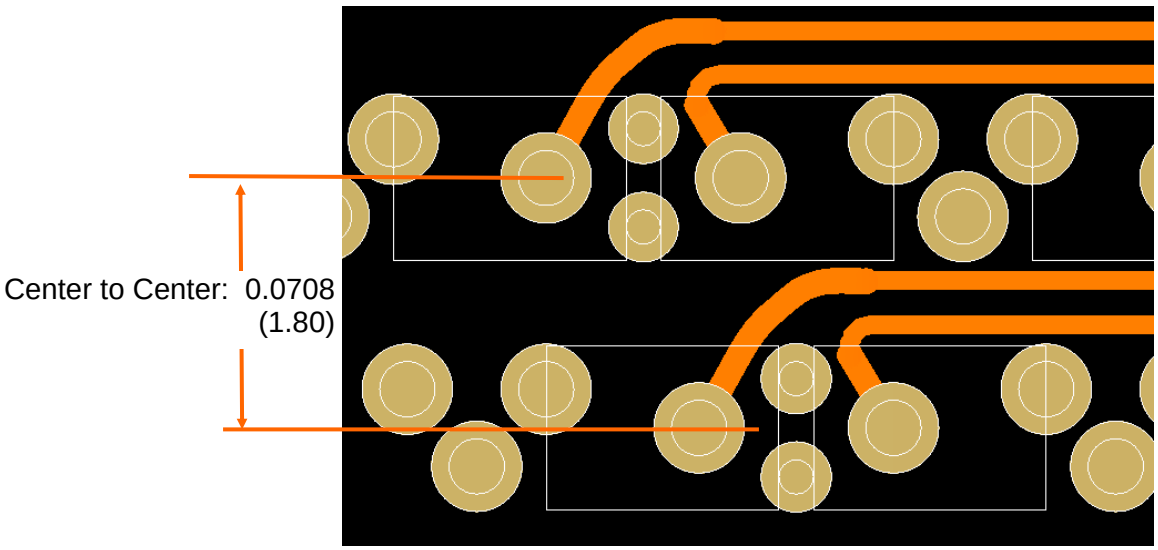


Figure 16: Example XCede® HD2 Daughtercard High Speed Differential Routing

Additionally, the use of the antipad shape shown on figure 16, placed directly below the routed diff pair, and making the un-coupled portion of the diff pair the corresponding width for the particular single ended impedance also greatly help with overall impedance matching and as mentioned common mode performance.

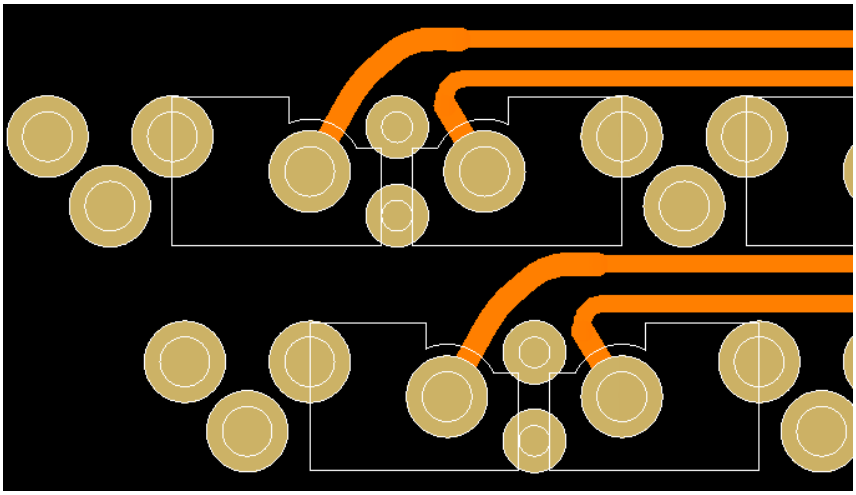


Figure 17: Example XCede® HD2 Daughtercard High Speed Differential Routing Advance

6.9 XCede® HD and XCede® HD Plus XCede® HD2 Example High Speed Differential Routing

For complete hole pattern dimensions please refer to the customer use drawings. The available space for routing is determined by the distance between antipads. This is an example and is not the minimum antipad required for manufacturability, but the antipad recommended for signal integrity.

Center to Center	**0.0708” (1.80)**
- AntiPad Diameter	**0.046” (1.17)**
= Resulting Space for Traces	**0.0248” (0.635)**
Line Width	**0.006” (0.15)**
Space Between Lines	**0.007” (0.18)**
Resulting Ground Plane Web Overhang on Each Side	**0.003” (0.076)**

Table 5: Example XCede® HD and XCede® HD Plus Daughtercard Routing Channel

Center to Center	**0.0708 (1.80)**
- AntiPad Diameter	**0.046 (1.17)**
= Resulting Space for Traces (including via clearance)	**0.017 (0.43)**
Line Width	**0.005(0.127)**
Space Between Lines	**0.007 (0.178)**
Resulting Ground Plane Web Overhang on Each Side	**0.0037 (0.094)**

Table 6: Example XCede® HD2 Daughtercard Routing Channel

Center to Center	**0.0708 (1.80)**
- AntiPad Diameter	**0.046 (1.17)**
= Resulting Space for Traces	**0.0248 (0.63)**
Line Width	**0.006 (0.152)**
Space Between Lines	**0.006 (0.152)**
Resulting Ground Plane Web Overhang on Each Side	**0.003 (0.076)**

Table 7: Example XCede® HD2 Backplane Primary (Horizontal) Routing Channel

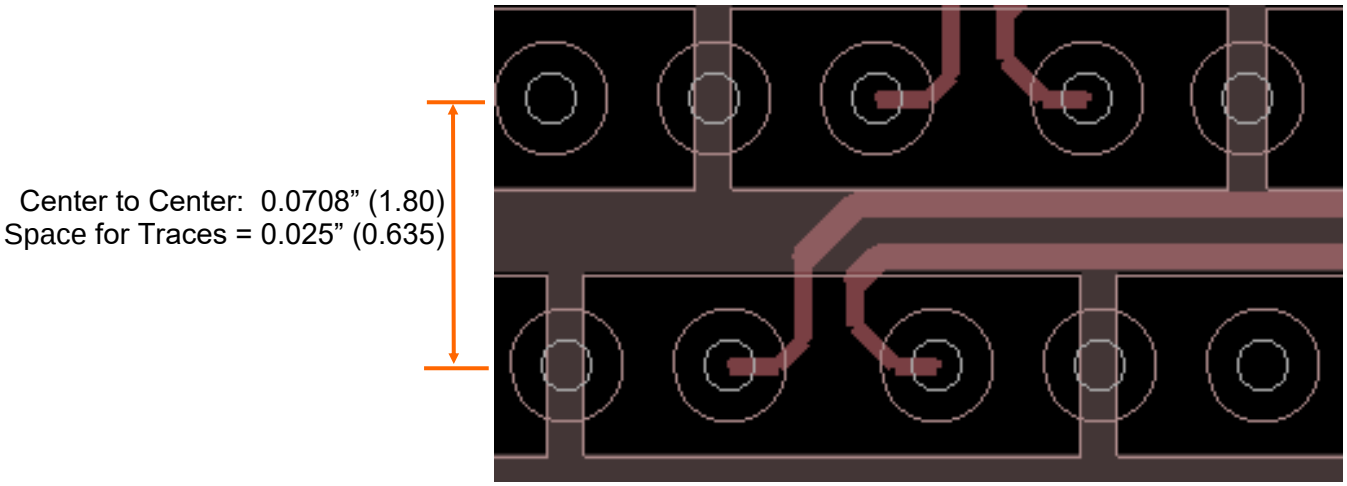


Figure 18: Example XCede® HD and XCede® HD Plus Daughtercard High Speed Differential Routing

6.9.1 Printed Circuit Board Skew Compensation

If the length of one net of a differential pair needs to be increased in order to achieve low skew within the pair, the following picture shows an example of how to achieve this goal.

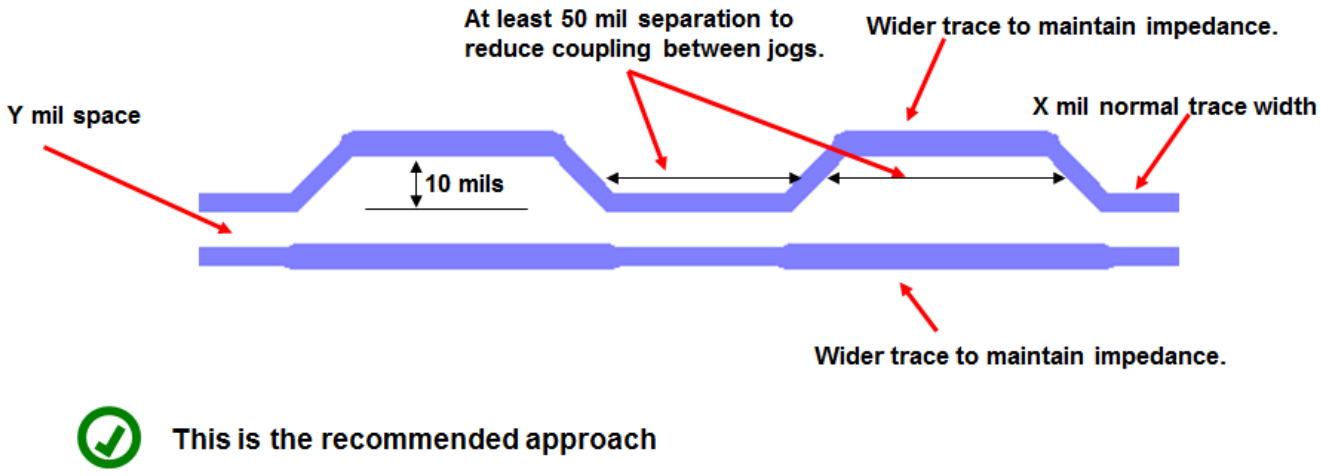


Figure 19: XCede® HD, XCede® HD Plus and XCede® HD2 Skew compensation recommended approach

7. Midplane Applications

The XCede HD connector can be used in a midplane application where vias are shared between front and rear cards. The examples below show two ways that the connector can share vias in a midplane application.

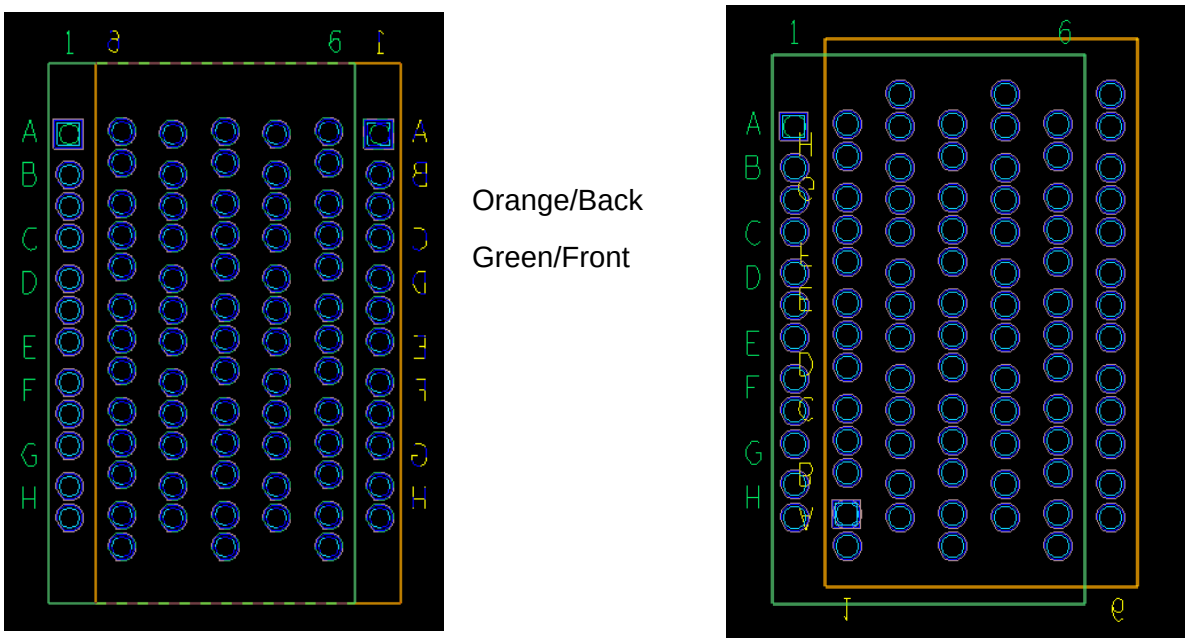


Figure 20: Example XCede® HD Midplane Connector