TB-2360

Paladin® HD / HD2 Routing Guidelines

Revision “C”

Specification Revision Status

Revision	SCR No.	Description	Initial	Date
“A”	S8922	Initial release	J Dunham	04/22/21
“B”	S10684	Drill size updated	S Demian	7/17/23
“C”	S11282	In-Line footprint added	J Dunham	5/16/24

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1. Scope

1.1 Purpose

The purpose of this technical bulletin is to describe the various required and recommended features of the printed circuit board footprint design and trace escape routing for optimal use of the Paladin HD connector. This document is intended to be used in conjunction with specified customer use drawings as called out below.

1.2 Printed Circuit Board Design Rules Reflect Available Printed Circuit Board Fabrication Capabilities

The technical capabilities of each individual printed circuit board manufacturer will determine the printed circuit design rules that are appropriate for acceptable yield manufacturing of a given size and complexity of printed circuit board utilizing a given insulating laminate material system. This document firstly outlines Amphenol rules that apply to all board designs using the Paladin HD interconnect. Secondly Amphenol board recommendations are intended to make designs more efficient for a given set of rules. Finally, detailed examples are shown, each of which proceeds from a particular set of technical PCB fabrication capabilities and electronic system performance requirements.

2. Important Considerations for Optimal Utilization of Paladin HD Connector

- Note: Corresponding pin-pair designations run A-B, C-D, E-F, G-H, etc. on the right angle connector footprint, and A-B, C-D, E-F, G-H, etc. on the BMA connector footprint (where applicable) of the mated connector.

- Pin-pair designations for direct ortho configurations are detailed in TB-2357.

- Provide for an exposed conductive surface ground layer on layer 1, free from solder mask or other insulating coating, as detailed in section 0. This will improve crosstalk isolation between signal pairs.

- The right angle connector footprint provides differential pair routing channels in both X and Y directions, i.e. it provides secondary differential pair routing channels. These secondary routing channels exist between pairs 4 and 5 and between pairs 8 and 9.

- Note: Since the electrical function, routing, and drill-to-inner-layer registration impact of all signal, ground, and ground shadow vias depends upon their outer conductive diameter, it is highly recommended that a specific metric or number drill be called out in the PCB fabrication documentation for the drilling of each plated press-fit hole or plated shadow via in the Paladin HD footprint.

- Back-drilling is recommended on signal vias to reduce physical stub and extend signal transmission bandwidth.

- Because Paladin HD uses compression signal springs to contact only the top surface of the PCB, there is no requirement on compliant pin working zone (and associated back-drilling) on signal vias. With the exception of the top (surface) layer of the board, all internal layers are available for high speed routing.

- The finished hole inner diameter of the press-fit ground holes need be controlled only for the top 0.70mm (0.028”) from the layer 1 side (Paladin HD Connector mounting side) of the PCB. See **Error! Reference source not found.** and Figure 2.

- The indicated ground shadow vias are important for the electrical performance of the Paladin HD Connector System. Unlike the press-fit holes, the specified positions and drilled diameters of these shadow vias may be adjusted to some degree to accommodate the particular fabrication and electrical requirements of a given application scenario. See section 0

- Ground shadow vias are allowed to be plated shut. The location and drill diameter determine connector performance.

- Signal vias are allowed to plated shut.

3. Design Rules and Manufacturability Guidelines for Press-Fit Holes

3.1.1 Press-Fit Hole Locations

Reference the customer use drawings.

3.1.2 Press-Fit Finished Hole Diameter Requirements

3.1.3 Description of Paladin HD press-fit pin (13.7 mil or 14.5 mil drill)

The "Atto" compliant pin is designed for a 0.35 mm (0.0137") or 0.37mm (0.0145") drill hole size plated through hole (PTH) with 0.57mm (0.0225") conductive pad on every ground layer. For plating considerations consult PCB fabricator or ATCS Application Engineering. This applies to signal and ground PTHs.

3.1.4 Dimensional Requirements for Press-Fit Holes in Compliant Pin Critical Working Zone

Finish Type	Copper thickness, in (mm) per side (1)	Drill size, in (mm) (2)	Typical Finish Thickness (3)	Finished Hole Size, in (mm) (4)
ENIG	0.0010 (0.0254) min 0.0025 (0.0635) max	0.0137 (0.35) OR 0.0145 (0.37)	3 micro inches Immersion gold min over 50 to 150 electroless nickel	0.0106±0.0015 (0.27±0.04)
ENEPIG	0.0008 (0.020) min 0.00275 (0.069) max	0.0137 (0.35) OR 0.0145 (0.37)	1 to 2 micro-inches immersion gold over 2 to 4 microinches of electroless Palladium over 50 to 150 microinches Nickel	0.0106±0.0015 (0.27±0.04)
Ni Au (Nickel-Gold)	0.0008 (0.020) min 0.00275 (0.069) max	0.0137 (0.35) OR 0.0145 (0.37)	30 micro-inches hard gold plating min over 53 to 210 micro inches Ni-Au composition	0.0106± 0.0015 (0.27±0.04)

Table 1: Copper Thickness Requirement and Finished Hole Inner Diameter

Notes (**Error! Reference source not found.**):

1. Copper thickness per side is an Amphenol requirement. The copper plating must be within specified range in **Error! Reference source not found.** according to the specific Finish Type selected by the end user. Copper plating at the knee of the hole is limited to a maximum of 10% above the average copper wall thickness measured in the working zone, see Figure 2 below, of the plated thru hole, and cannot exceed the MAX copper plating thickness specified in **Error! Reference source not found.**.
2. Drill size is an Amphenol requirement. Amphenol requires either drill to be used as outlined in **Error! Reference source not found.**. The drill size should be selected by the PCB fabricator to reach the Finished Hole Size as outlined in Table 1. The drill size specified does not include a tolerance nor does it include a drilled hole tolerance. These tolerance allowances are included in the overall tolerance outlined in the Finish Hole Size tolerance reference range.
3. Typical Finish Thickness is an Amphenol reference value of all finishes except ENIG (Nickel plating thickness for ENIG finish is a requirement). Amphenol highlights the reference values on these finishes as

a guideline for processing and inspection of PCB holes. Actual finish thicknesses will vary depending on the finish type selected by the end used design guidelines.

4. Finish Hole Size is an Amphenol nominal value. The Finish Hole Size tolerance for each finish type accounts for the accumulation of tolerances in the actual Drill Hole Diameter as a result of using the specified drills noted in the table above and Finish Thickness over the range of holes in a connector-hole pattern on a PCB. Cu thickness, finish plating thickness, and Drill Size must be adhered to per Amphenol's requirements in this document, but not cumulatively exceeded where these tolerance buildups exceed the finish hole requirements called out.

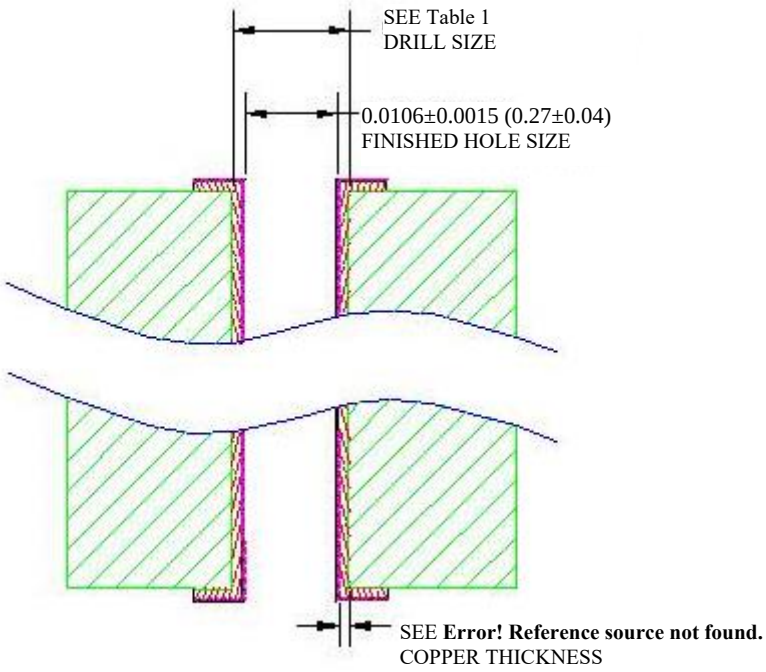


Figure 1: Paladin HD Drill and Finished Hole Size

3.1.4.1 Compliant Pin Critical Working Zone

The “Critical Working Zone” shown in Figure 2 is defined as the compliant working zone where the plated through hole requirements must meet the specifications defined within this document. In the “Non Critical Zone”, the plated through hole is allowed to go below the minimum required finish hole size for non-midplane applications. Back drilling is allowed in the “non-critical zone” only.

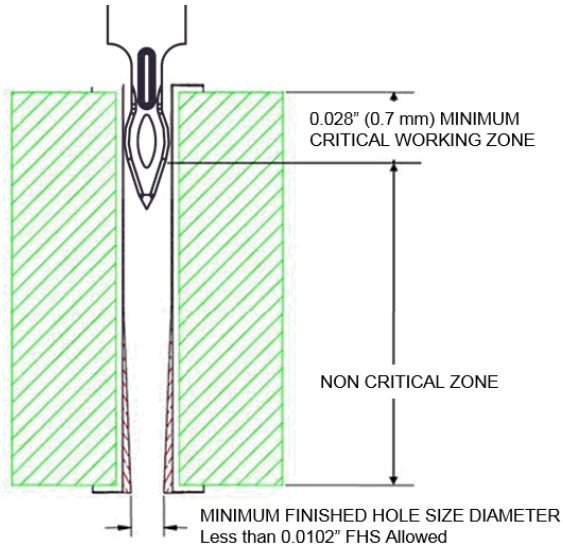


Figure 2: 0.0137” or 0.0145” Compliant Pin Critical Working Zone

4. Signal Drills and Signal Surface Pads – conventional 2.4mm x 2.4mm foot-print

Please refer to customer drawings for relative size and placement of signal drills, signal pads and ground vias.

Signal drill vias are specified at 0.23mm drill (0.0091inches). Because the signal vias do not accept a press fit pin, the vias can be plated shut. Signal vias are designated as #1 (two places per differential pair).
Signal surface pads – where the connector signal spring meets the PCB is labeled as #2 (two places per differential pair). ***These signal surface pads require a noble metal plating with geometries and locational tolerances specified in Paladin HD Customer Use drawings.***

And as reference, ground vias (accepting press fit pins) are designated as #3 (four places per differential pair).
Ground shadow vias are designated #4.

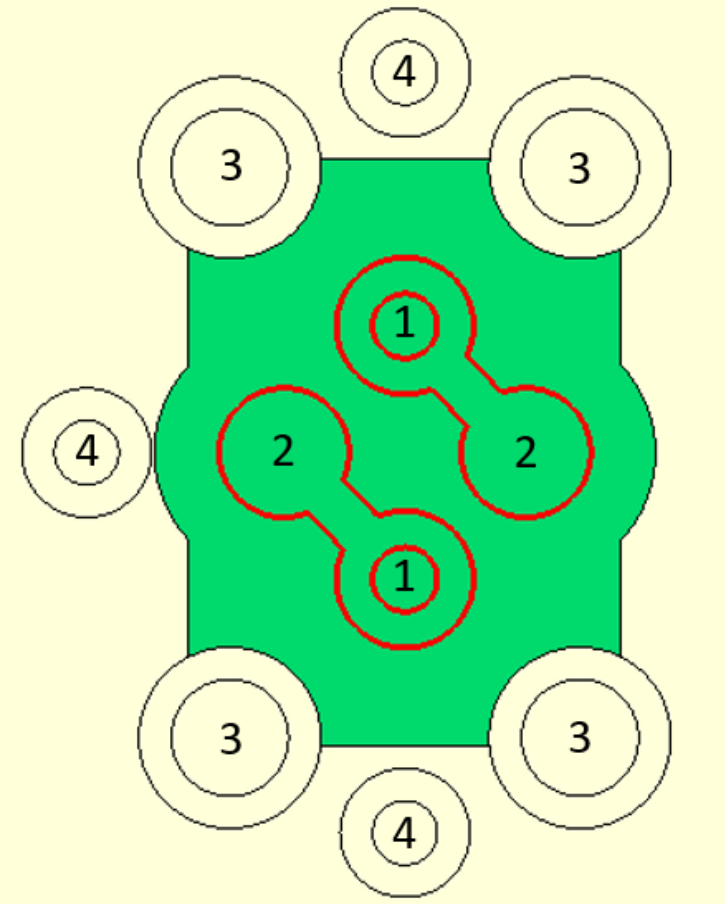


Figure 3: Paladin HD Signal Drills, Surface Pads, Ground Pin Accepting PTH, and Ground Shadow Vias

4.1 Minimum PCB Thickness

Minimum PCB thickness is 1.0mm (0.039 inches). Note that for boards less than 1.25mm (0.049 inches) thick the press-fit pins may protrude from the rear-side of the board.

4.2 Conductive Surface Layer – conventional 2.4mm x 2.4mm foot-print

It is required that the top surface layer which the Paladin HD connector is pressed into has a conductive ground layer free from insulating coating in the connector footprint region. See Figure 4.

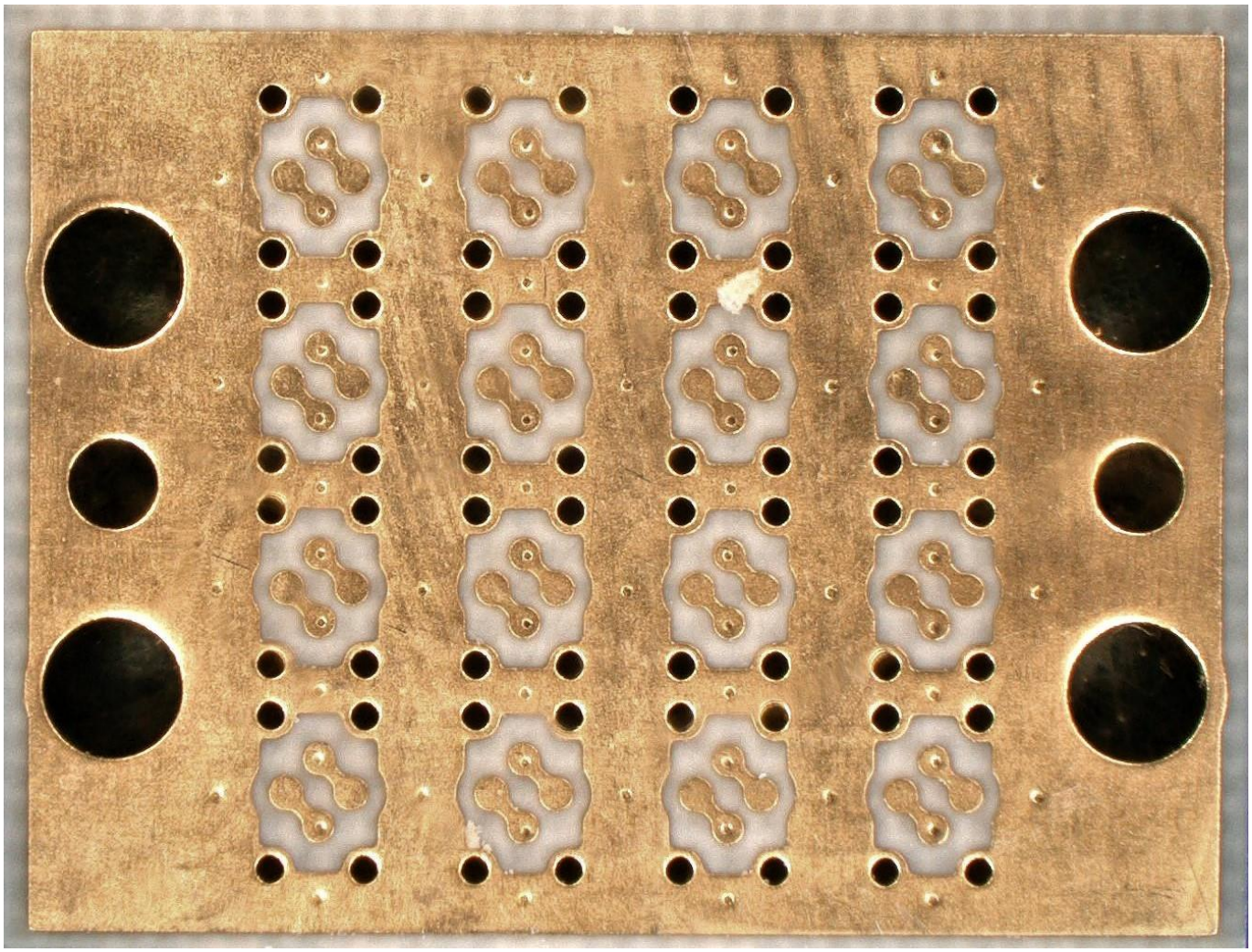
4.3 Surface Flatness of Connector Pattern

It is required that each individual connector footprint pattern maintain a maximum flatness of 0.08 mm. Each connector footprint pattern is defined as an individual module connector with guide endcaps at each end, or multiple module connectors with middle joining guides and guide endcaps on each end.

4.3.1 Surface Flatness of Signal Pad

It is required that each individual signal pad have a flatness within 0.025 mm (max dimple of 0.025).

Figure 4: Conductive Ground Layer Example on Connector Footprint



4.4 Anti-pad Considerations – conventional 2.4mm x 2.4mm foot-print

The Paladin HD interconnect has four anti-pad shapes utilized on specified layers for intended functions.

4.4.1 Layer 1 (Surface Anti-pad) – conventional 2.4mm x 2.4mm foot-print

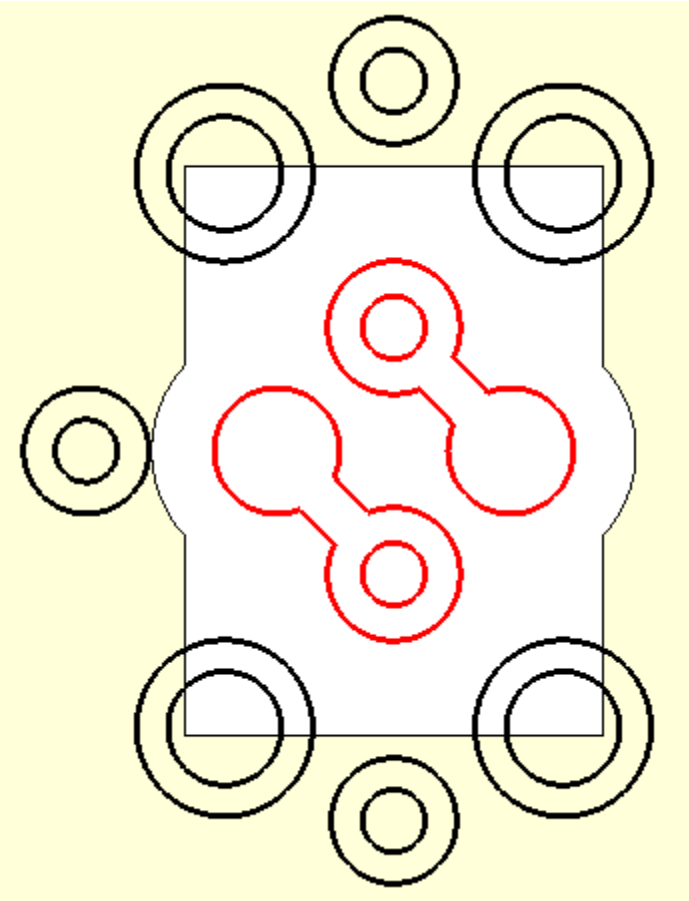


Figure 5: Paladin HD Footprint Layer 1 Anti-pad Shape

4.4.2 Layer 2 (Depth Controlled) – conventional 2.4mm x 2.4mm foot-print

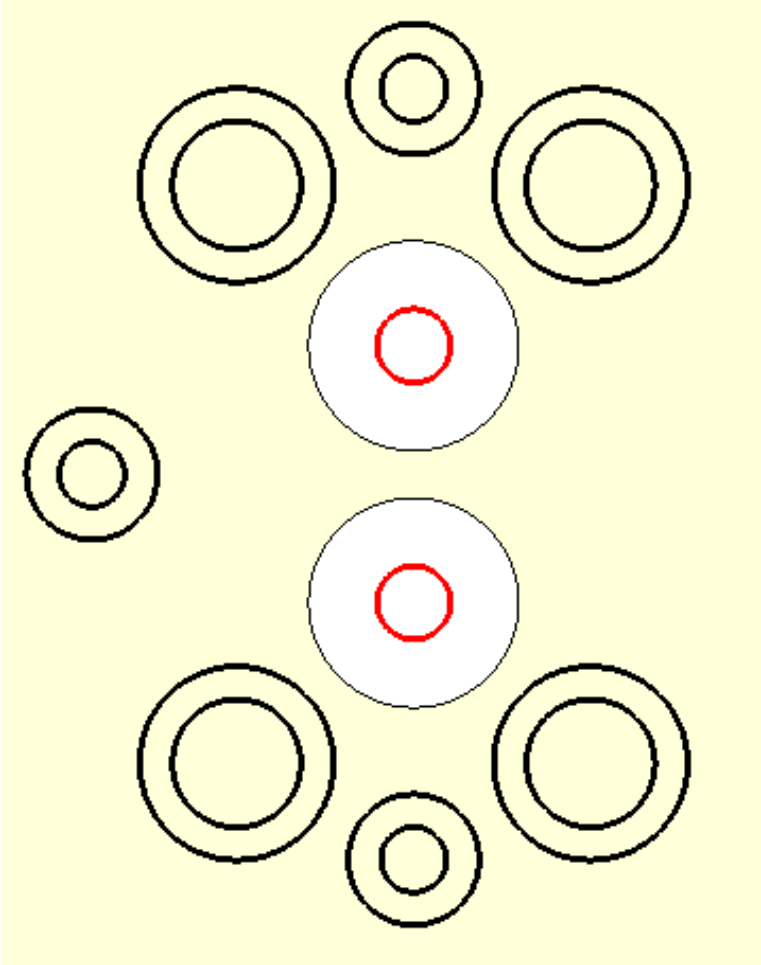


Figure 6: Paladin HD Footprint Layer 2 Anti-pad Shape

~~4.3.3~~ 4.4.3 Open Anti-pad – conventional 2.4mm x 2.4mm foot-print

The open anti-pad shape is rectangular and is used on all ground layers that are not otherwise specified. This anti-pad shape should be used on each ground layer between plane Layer 2, two layers above the breakout layer, two ground layers below the breakout layer, and each ground plane layer deeper into the PCB until the bottom layer.

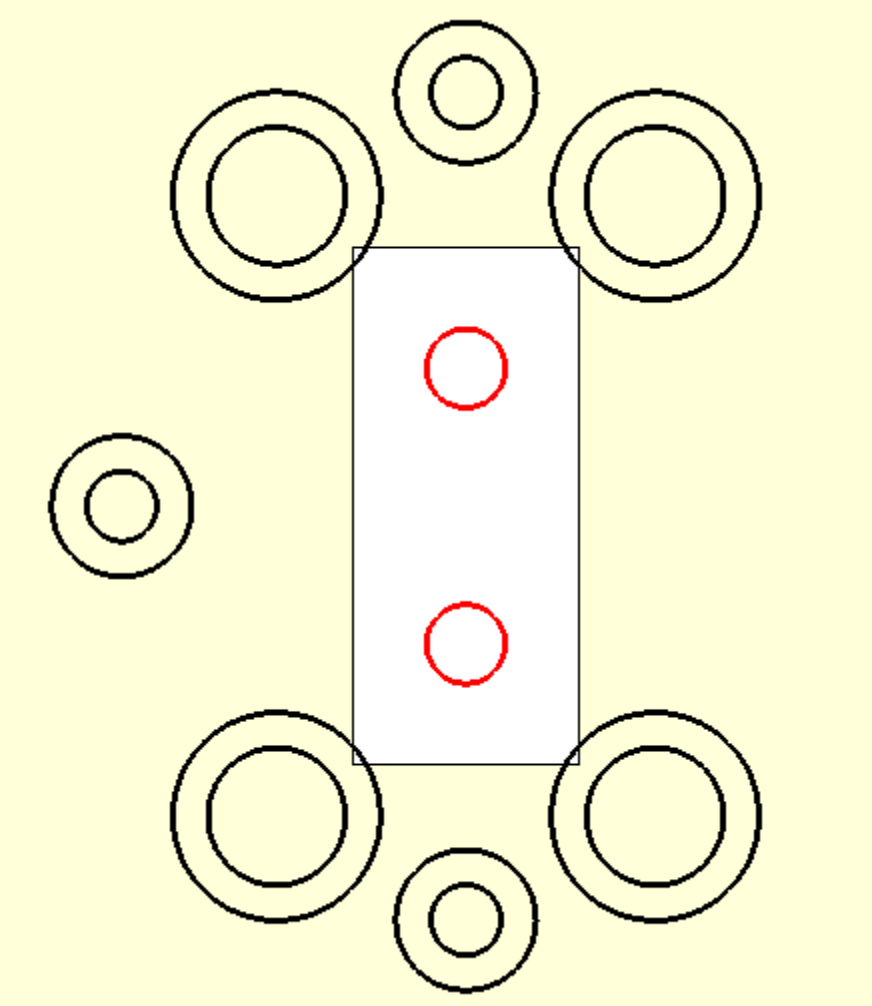


Figure 7: Paladin HD Footprint Open Anti-pad

4.43.4 Breakout Coupling Anti-pad – conventional 2.4mm x 2.4mm foot-print

The breakout coupling anti-pad shape is specified for the ground planes above and below the breakout layer.

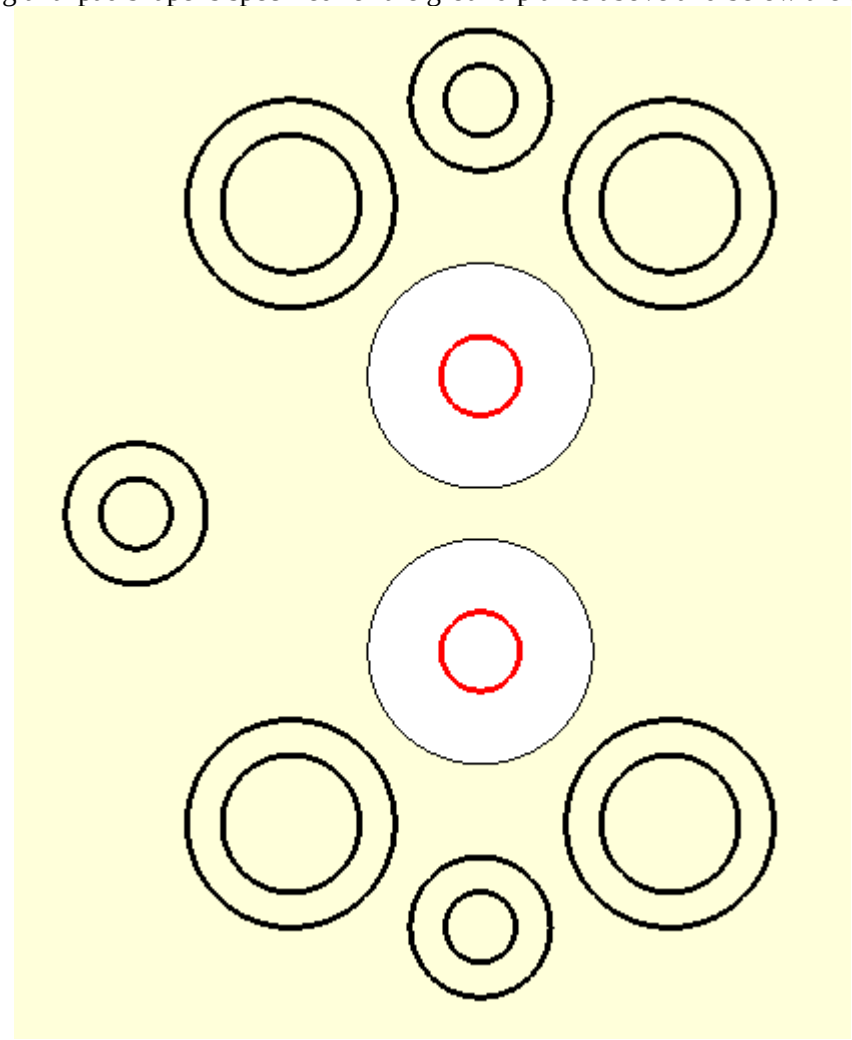
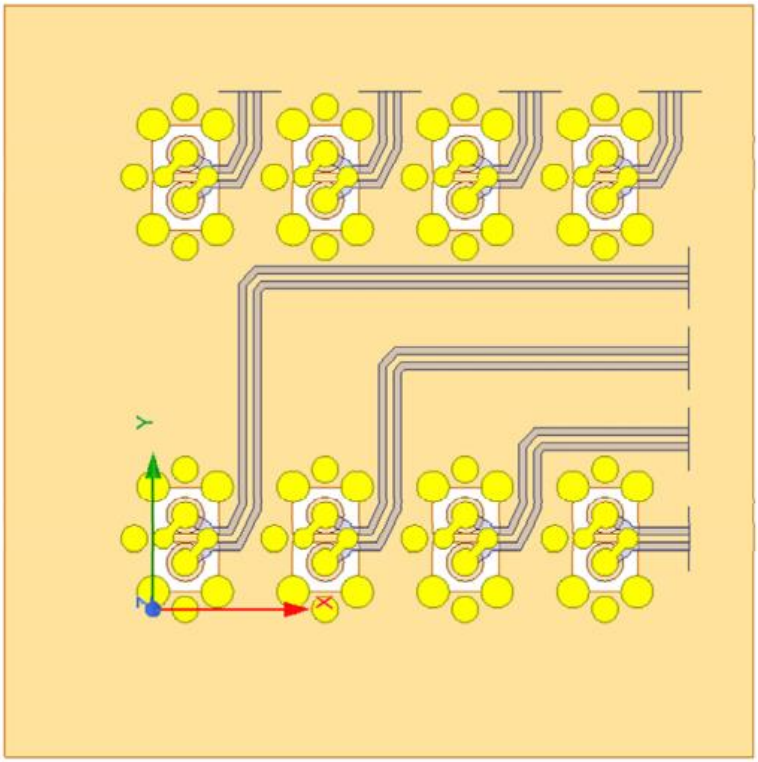


Figure 8: Paladin HD Footprint Breakout Coupling Anti-pad

4.5 Trace Routing - Paladin HD2, 2.4mm x 2.4 version

The PHD2 footprint has been designed for a 15 mil wide routing channel, based on via location and typical PCB DFM guidelines. Larger routing channels may be possible with slight changes to via locations and DFM guidelines.



5-5-5 mil diff pairs

Maintain 8mil min D2M

Maintain 23.7mil pair to pair space

5. Signal Drills and Signal Surface Pads, Paladin HD2, 2.4mm x 2.8mm “In-Line” version.

Signal vias are designated as #1 (two places per differential pair). Signal drill vias are specified at 0.20mm drill (0.0079inches). Larger dill sizes may be possible when evaluating the tradeoffs between routing channel needs and PCB DFM (design for manufacturability) requirements. These vias are intended to be via in pad (VIPPO).

Signal surface pads – where the connector signal spring meets the PCB is labeled as #2 (two places per differential pair). ***These signal surface pads require a noble metal plating with geometries and locational tolerances specified in Paladin HD Customer Use drawings.***

Ground vias (accepting press fit pins) are designated as #3 (four places per differential pair). The drill size and finished hole size requirements are listed in table 1, and on the applicable customer use drawings.

Ground shadow vias are designated #4. Ground shadow via drills are specified at 0.20mm drill (0.0079inches). Larger dill sizes may be possible when evaluating the tradeoffs between routing channel needs and PCB DFM (design for manufacturability) requirements. These vias may be through vias or via in pad (VIPPO).

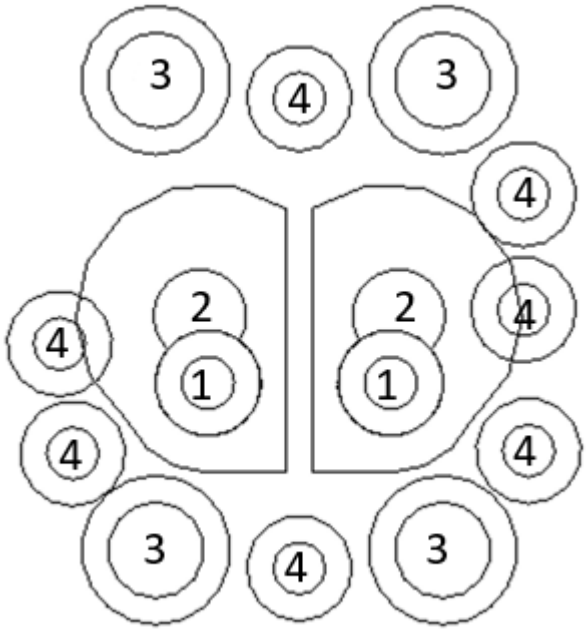
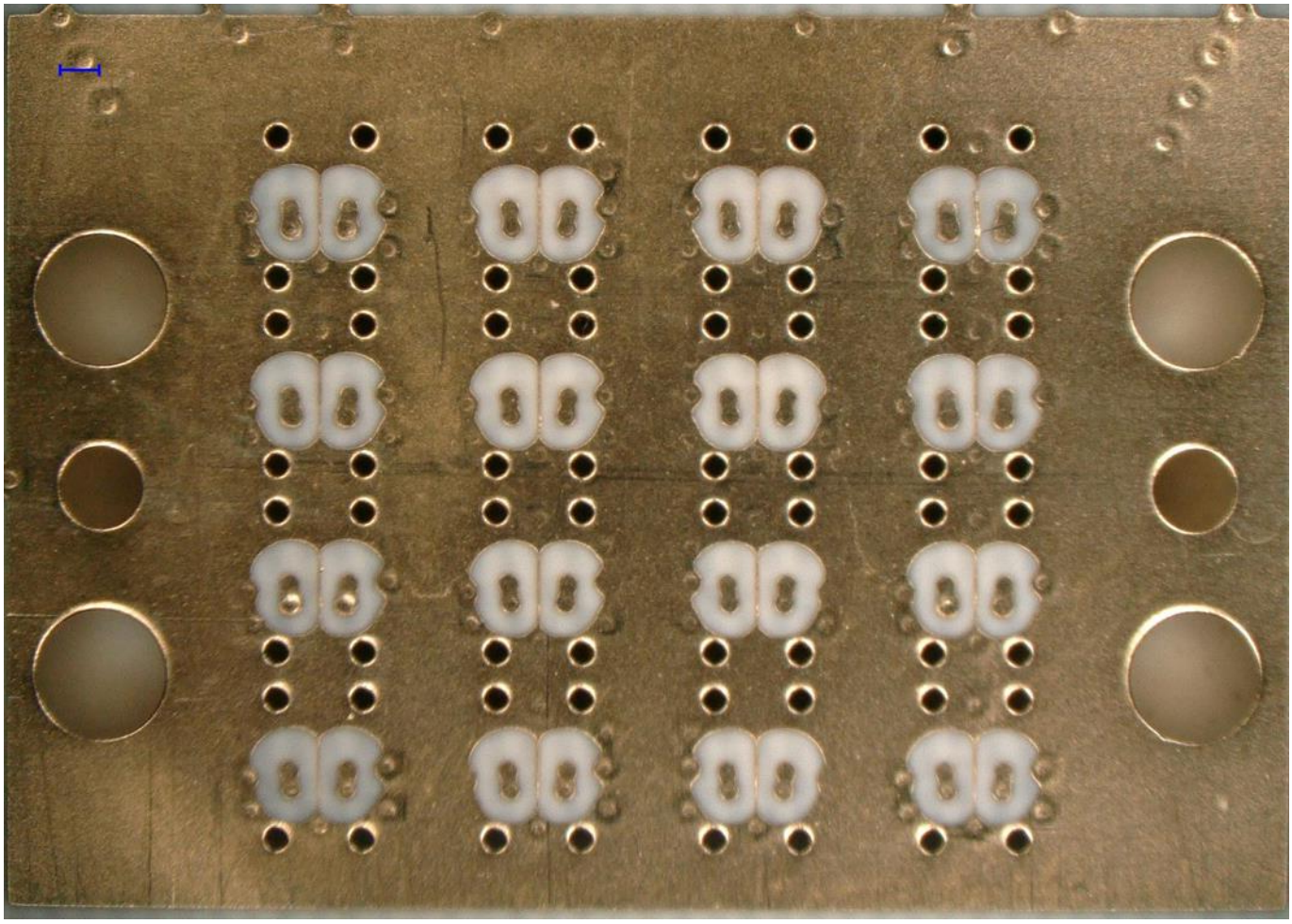


Figure 9: Paladin HD Signal Drills, Surface Pads, Ground Pin Accepting PTH, and Ground Shadow Vias

5.1 Conductive Surface Layer Paladin HD2, 2.4mm x 2.8mm “In-Line” version

It is required that the top surface layer which the Paladin HD connector is pressed into has a conductive ground layer free from insulating coating in the connector footprint region. See Figure 4.

Figure 10: Conductive Ground Layer Example on “In-Line” Connector Footprint



5.2 Anti-pad Considerations Paladin HD2, 2.4mm x 2.8mm “In-Line” version

The Paladin HD2 interconnect has anti-pad shapes utilized on specified layers for intended functions.

5.3 Layer 1 (Surface Anti-pad) Paladin HD2, 2.4mm x 2.8mm “In-Line” version

The top layer antipad is constructed with two overlapping shapes. The first shape is an oval antipad centered on the through via’s. The size of this shape should be confirmed with simulation. A good starting point would be a 27mil (0.69mm) oval. The second shape is a circle centered on the pressure mount landing pad. The size of this shape is 36mil (0.91mm). The last step in the addition of a 4mil (0.10mm) wide copper strip place in the center of the shape as shown in figure 5.

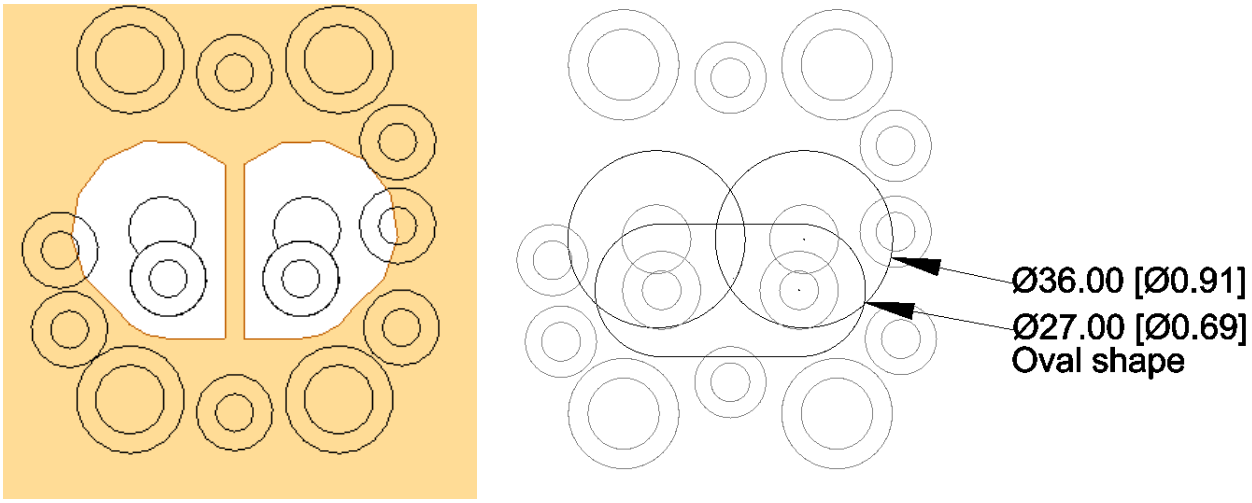


Figure 11: Paladin HD2 Footprint Layer 1 Anti-pad Shape

5.4 Open Anti-pad - Paladin HD2, 2.4mm x 2.8mm “In-Line” version

The open anti-pad shape can be round or oval and is used on all ground layers that are not otherwise specified. The exact size to be determined based on material choice and impedance requirements.

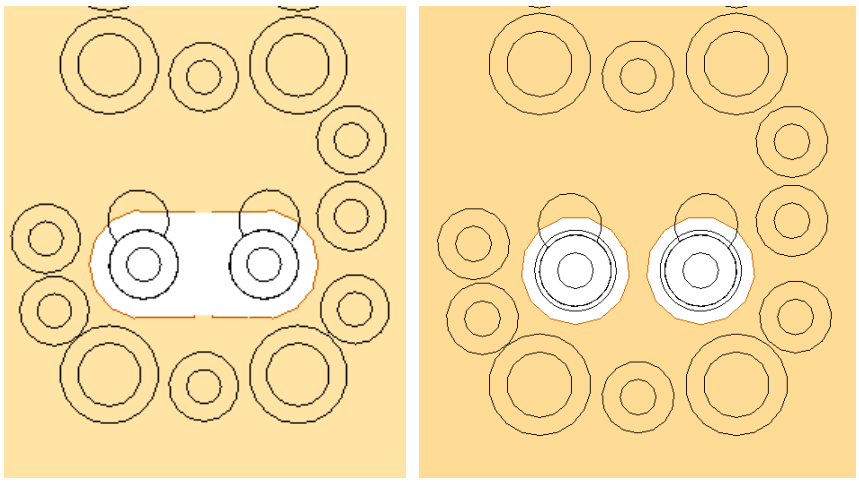


Figure 12: Paladin HD Footprint Open Anti-pad

5.5 Breakout Coupling Anti-pad - Paladin HD2, 2.4mm x 2.8mm “In-Line” version

The breakout coupling anti-pad shape is specified for the one ground plane above and the one ground plane below the breakout layer. The exact size to be determined based on material choice and impedance requirements. A 4 mil (0.1mm) wide copper strip is added to the center of the shape. *This strip is critical to high speed applications.*

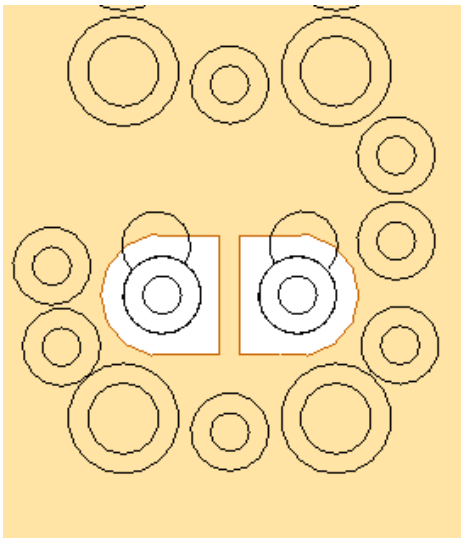


Figure 13: Paladin HD Footprint Breakout Coupling Anti-pad

5.6 Trace Routing - Paladin HD2, 2.4mm x 2.8mm “In-Line” version

The PHD2 footprint has been designed for a 15 mil wide routing channel, based on via location and typical PCB DFM guidelines. Larger routing channels may be possible with slight changes to via locations and DFM guidelines.

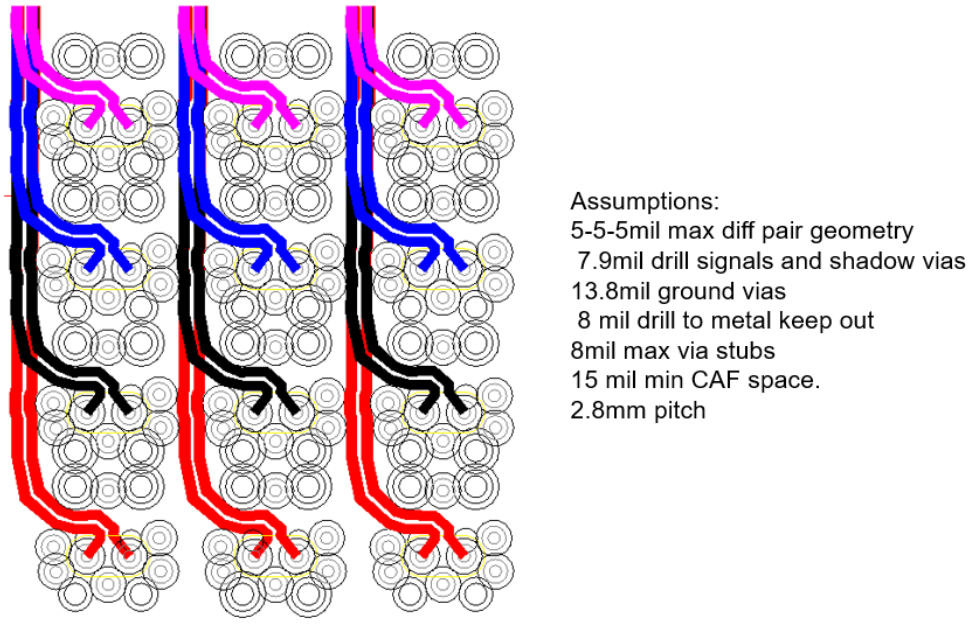


Figure 14: Paladin HD2 Trace Routing

5.7 Trace routing breakout example - Paladin HD2, 2.4mm x 2.8mm “In-Line” version

Using the routing gap, located between pairs 4 & 5 and pairs 8 & 9, the total number of routing layers needed can be reduced. Refer to the below example.

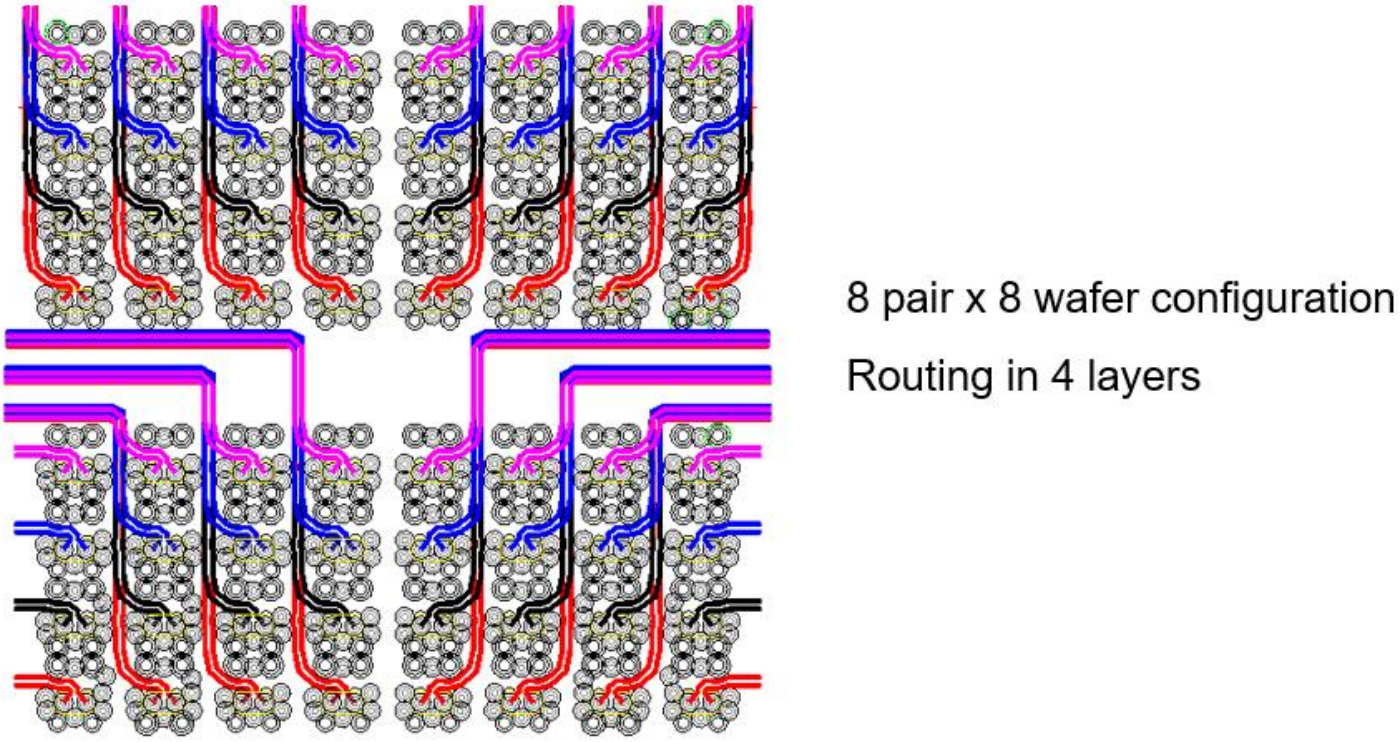


Figure 15: Paladin HD2 Trace Routing Example

6. Signal Drills and Signal Surface Pads, Paladin HD2, 2.4mm x 2.8mm Male Header Backplane version.

Signal vias are designated as #1 (two places per differential pair). Signal drill vias are specified at 0.20mm drill (0.0079inches). Larger dill sizes may be possible when evaluating the tradeoffs between routing channel needs and PCB DFM requirements. These vias are intended to be via in pad (VIPPO)

Signal surface pads – where the connector signal spring meets the PCB is labeled as #2 (two places per differential pair). ***These signal surface pads require a noble metal plating with geometries and locational tolerances specified in Paladin HD Customer Use drawings.***

Ground vias (accepting press fit pins) are designated as #3 (four places per differential pair). The drill size and finished hole size requirements are listed in table 1, and on the applicable customer use drawings.

Ground shadow vias are designated #4. Ground shadow via drills are specified at 0.20mm drill (0.0079inches). Larger dill sizes may be possible when evaluating the tradeoffs between routing channel needs and PCB DFM requirements. These vias may be through via’s or via in pad (VIPPO).

6.1 Conductive Surface Layer Paladin HD2, 2.4mm x 2.8mm “In-Line” version

It is required that the top surface layer which the Paladin HD connector is pressed into has a conductive ground layer free from insulating coating in the connector footprint region. See Figure below.

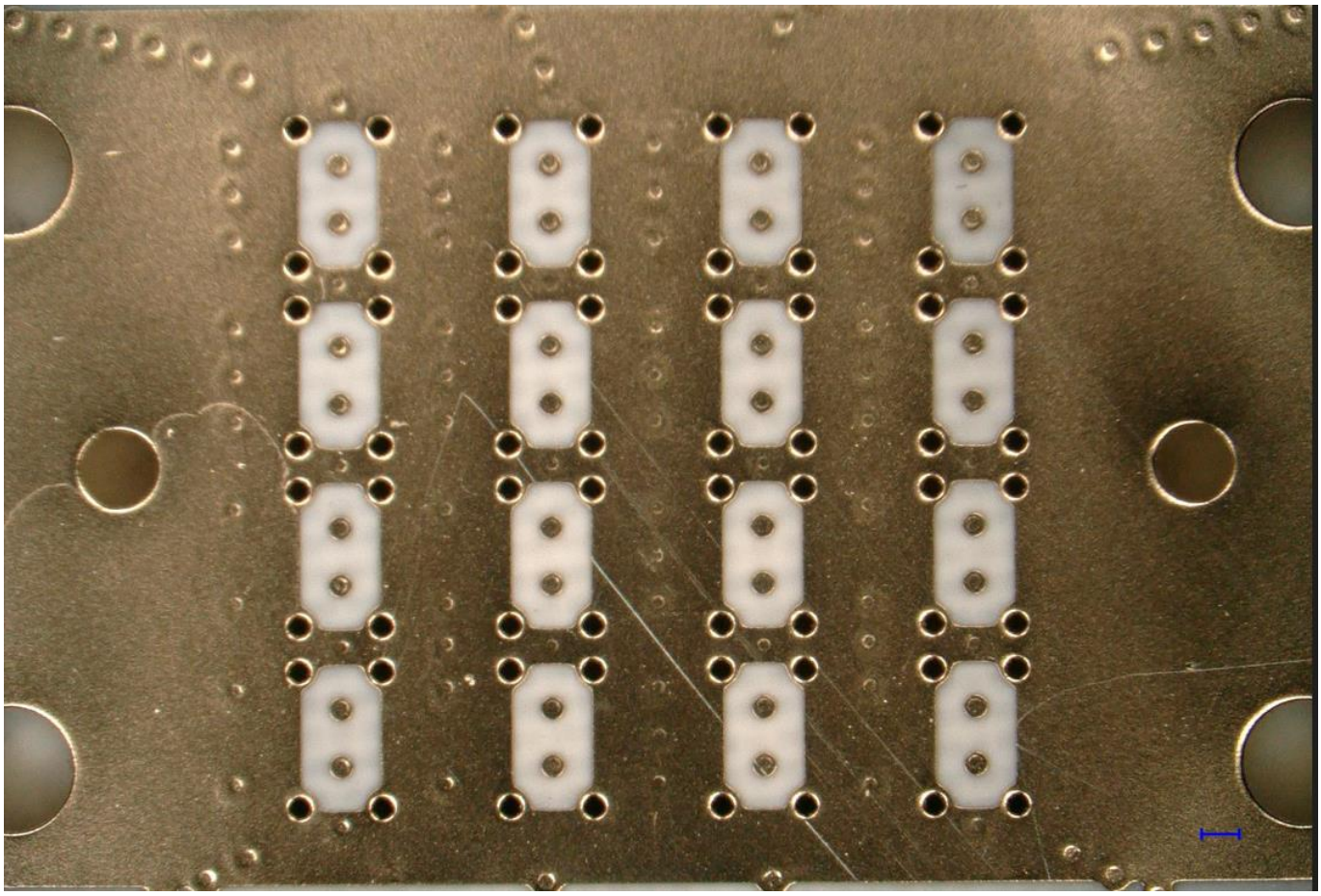


Figure 10: Paladin 2.8mm Backplane Conductive Ground Layer

General Recommendations

6.2 Surface Traces

Surface traces are not recommended in the region of the connector footprint on the primary side where the connector is attached.

6.3 Shadow Vias

Ground shadow vias are important for the electrical performance of the Paladin Connector System. Unlike the press-fit vias, the precise position and drill diameter of these shadow vias may be adjusted to some degree to accommodate the particular fabrication and electrical requirements of a given application. There is a minimum copper wall thickness requirement of 0.025mm (0.001”), however there is no maximum wall thickness requirement (may be plated shut). The ground via diameter requirement varies depending on the specific application. Contact your local field applications engineer for support on optimizing the shadow via geometry.

6.4 Mounting holes

It is recommended that the mounting holes that accept mechanical screws and posts are to be plated. Mounting holes are generally located on the ends of the connector. For connectors other than direct – orthogonal applications, contact Amphenol Engineering for mounting hole best practices.

7. Signal Integrity Aspects of Footprint Design

7.1 Surface Conductive Layer

It is required that the top surface layer which the Paladin HD connector is pressed into has a conductive ground layer free from insulating coating in the connector footprint region. This is important for optimizing signal transmission and reducing reflections and crosstalk. See Figure 4.

7.2 Relative Dielectric Constant of Laminate Material

Note that different laminate insulating materials have differing dielectric constant values. The dielectric constant value will affect the characteristic impedance of the differential plated holes, trace escape, and routed traces. For this reason, it is usual to adjust such parameters as anti-pad size, location and drill diameter of ground shadow vias, trace escape configuration, trace width, and dielectric thicknesses to optimize the electrical signal integrity performance.

7.3 Location and Finished Plated Hole Sizes for Signal Vias and Compression Contacts

The signal compression contact pads are specified and must match the pattern of the compression contacts of the corresponding connector. The surface pad that accepts the spring must be plated with a noble metal. The diameter of these contact surface pads is important for the proper functioning of the compression connector attachment and should be controlled as per requirements documented. The electrical characteristics of these geometries is determined by the surface pad geometry, the surface connection between the pad and the via, and the drill diameter, which should therefore be specified (either metric or numbered drill) for drilling these holes. The drilled signal vias can be plated shut.

7.4 Back-drilling

Signal plated through holes should be back-drilled to reduce the length of the electrical stub formed in the region between the signal escape layer and the bottom PCB layer. Stub resonances are undesirable because they increase return loss and reduce signal transmission bandwidth.

7.5 Always Remove Non-Functional Pads on Signal Plated Through Holes

Non-functional pads on signal plated through holes are undesirable because they typically lower the characteristic impedance below desired values. In typical applications, the only pads attached to a signal plated through hole are those on the primary connector attach surface, and the internal escape layer where there are pads to attach the signal plated through hole to signal traces.

7.6 Location and Finished Plated Hole Sizes for Ground Press-Fit Holes

The ground press-fit contacts are specified and must match the pattern of press-fit contacts of the corresponding connector. The internal diameter of these finished plated holes is important for the proper functioning of the press-fit connector attachment and should be controlled as per requirement for the specified working range depth from the connector side of the board. The electrical characteristics of these plated holes, on the other hand, is determined by the drill diameter, which should therefore be specified (either metric or numbered drill) for drilling these holes.

7.7 Diameter and Location of Ground Shadow Vias

Note that there is no finished hole size requirement for these vias and they can be plated shut. There is some degree of flexibility in the location and drill diameter used for these vias. They perform important electrical functions in reducing footprint crosstalk and controlling characteristic impedance. Note that their electrical characteristics depend on the diameter of the drill used, and therefore a specific drill size (either metric or numbered drill) should be specified for drilling these vias. These shadow vias can be plated shut.

Appendix A: Definitions and Considerations

Foils Thickness or Copper Weight
Consider copper weight when routing. Higher weights will impact minimum trace widths. Copper foil is measured in ounces (or weight). Common copper weights are 0.5 ounces, 1 ounce, 1.5 ounces and 2 ounces (3 ounces up to 10 ounces are available for special order). 1 ounce = 0.0014”, 1.5 ounces = 0.0021”, 2 ounces = 0.0028”.

Pads/Lands/Annular Ring
A pad is the support around a hole. A specification describing an annular ring of 0.005” means the amount of the pad left around the hole after processing.

Spacing
Spacing is the space between two electrical connections; it can be between two lines, two pads, a line and a pad etc.

Trace/Circuit/Line Width/Lines/Conductor
These are different terms for a connection. If you see the term 0.008” lines, it means the electrical connection from one point to another will measure 0.008” width.

BMA
Backplane Module Assembly Connector.

RAF
Right Angle Female Connector.

DOM
Direct orthogonal male connector.

Trace Centering
Center all traces between holes to optimize spacing.

Non-Functional Pads
A non-functional pad is a signal pad around a plated drilled hole that does not connect to a functioning signal trace.

Characteristic Impedance
Characteristic Impedance is a high frequency electrical property of a signal transmission path modeled as a transmission line. A differential pair signal path has both a differential and common-mode characteristic impedance. In general, it is advantageous for efficient signal transmission to appropriately match the characteristic impedances of various successive portions of a signal transmission path. Consider characteristic impedance when designing to ensure line widths will meet requirements. Please contact ATCS Application Engineering for impedance calculations.